ZNA134

CCIR/EIA TV SYNCHRONISING PULSE GENERATOR

FEATURES

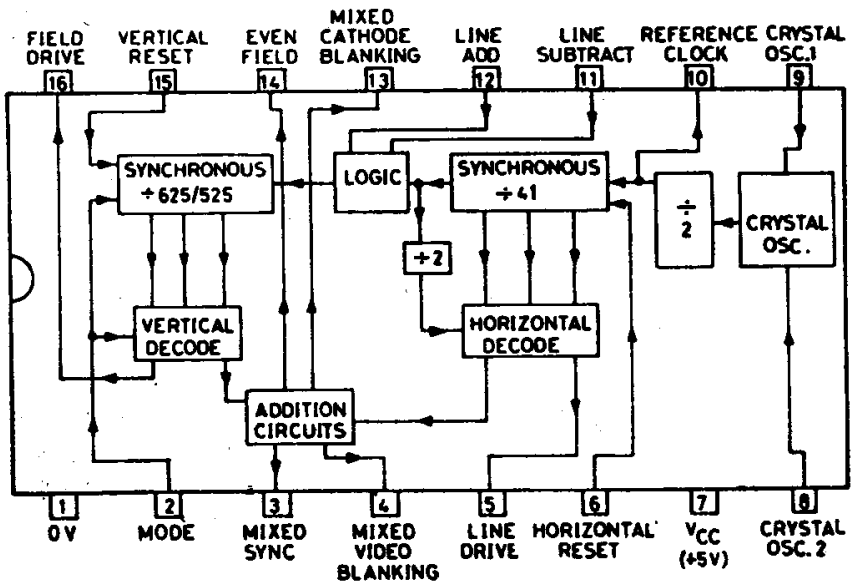
- 625 and 525 line standards.
- CCIR and EIA standard outputs.
- Single 5 volt supply, fully TTL compatible.
- Easy synchronising between generators.
- Direct reset to vertical and horizontal counters.
- Facility for adding and subtracting lines.
- Automatic interlacing.
- On chip oscillator (requiring external crystal).
- Can be driven with an external oscillator.
- Field reference output.

GENERAL DESCRIPTION

The ZNA134 integrated circuit utilises a 2.5 MHz* crystal to generate all the horizontal, vertical, mixed blanking and synchronising pulses necessary for raster generation in 625 or 525 line commercial, industrial or military television systems. The synchronous dividers and decoding logic employed within the unit ensure perfect interlace, together with spike-free output waveforms having precisely defined relative positions and pulse widths. The device is contained in a 16 pin D.I.L. and can be selected to operate over the military temperature range.

*Dependent on line system used, series resonant.

SYSTEM DIAGRAM



DG16

CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Maximum value
Supply Voltage	7 volts
Input Voltage	5 volts
Operating Temperature Range	0°C to +70°C*
Storage Temperature Range	−65°C to +150°C

*Also available over wider range on request.

OPERATING CHARACTERISTICS

(over recommended temperature range)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		4.75	5.0	5.25	Volts
Supply Current	I_S		–	100	–	mA
High-level Input Voltage	V_{IH}		2.4	–	–	Volts
Low-level Input Voltage	V_{IL}		–	–	0.8	Volts
High-level Input Current	I_{IH}	V_{CC} = 5V, V_I = 2.4V (See Note 1)	–	–	40	μA
Low-level Input Current	I_{IL}	V_{CC} = 5V, V_I = 0 V. (See Note 1)	−40	–	–	μA
High-level Output Voltage	V_{OH}	V_{CC} = 5V, $I_{source} \leqslant 80\mu A$ (See Note 2)	2.4	–	–	Volts
Low-level Output Voltage	V_{OL}	V_{CC} = 5V, $I_{sink} \leqslant$ 3.2 mA (See Note 2)	–	–	0.5	Volts
Clock frequency	f_{clock}	625 lines, Mode = '1' 525 lines, Mode = '0'	– –	2.56250 2.5830	– –	MHz MHz
External Oscillator Pulse Width	t_w	-ve going pulse, 625/525 lines	150	200	250	ns

Note 1

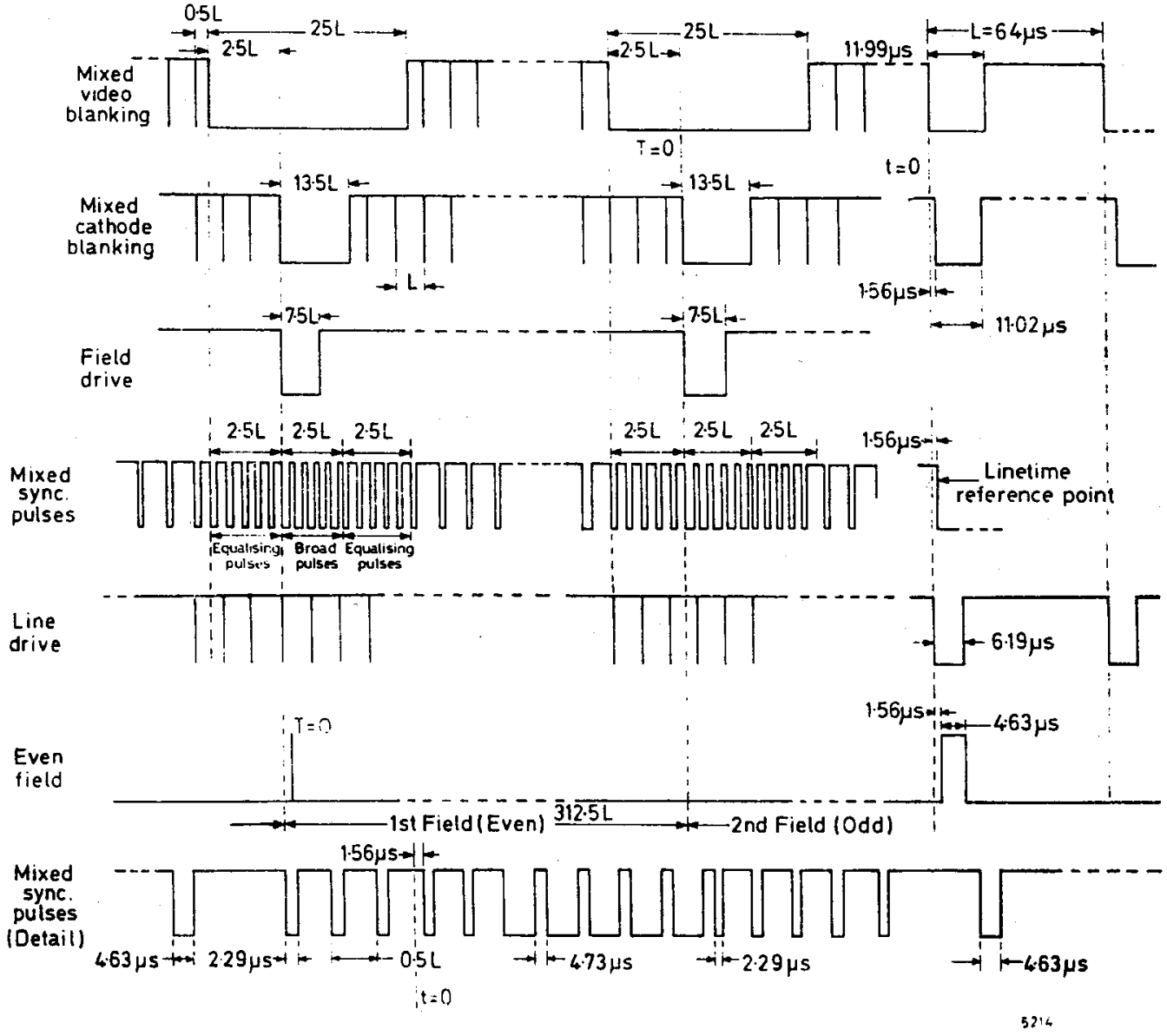
Input conditions only apply to mode, horizontal reset, vertical reset, line subtract and line add. For input conditions of oscillator inputs C.0.1, C.0.2, see applications section.

Note 2

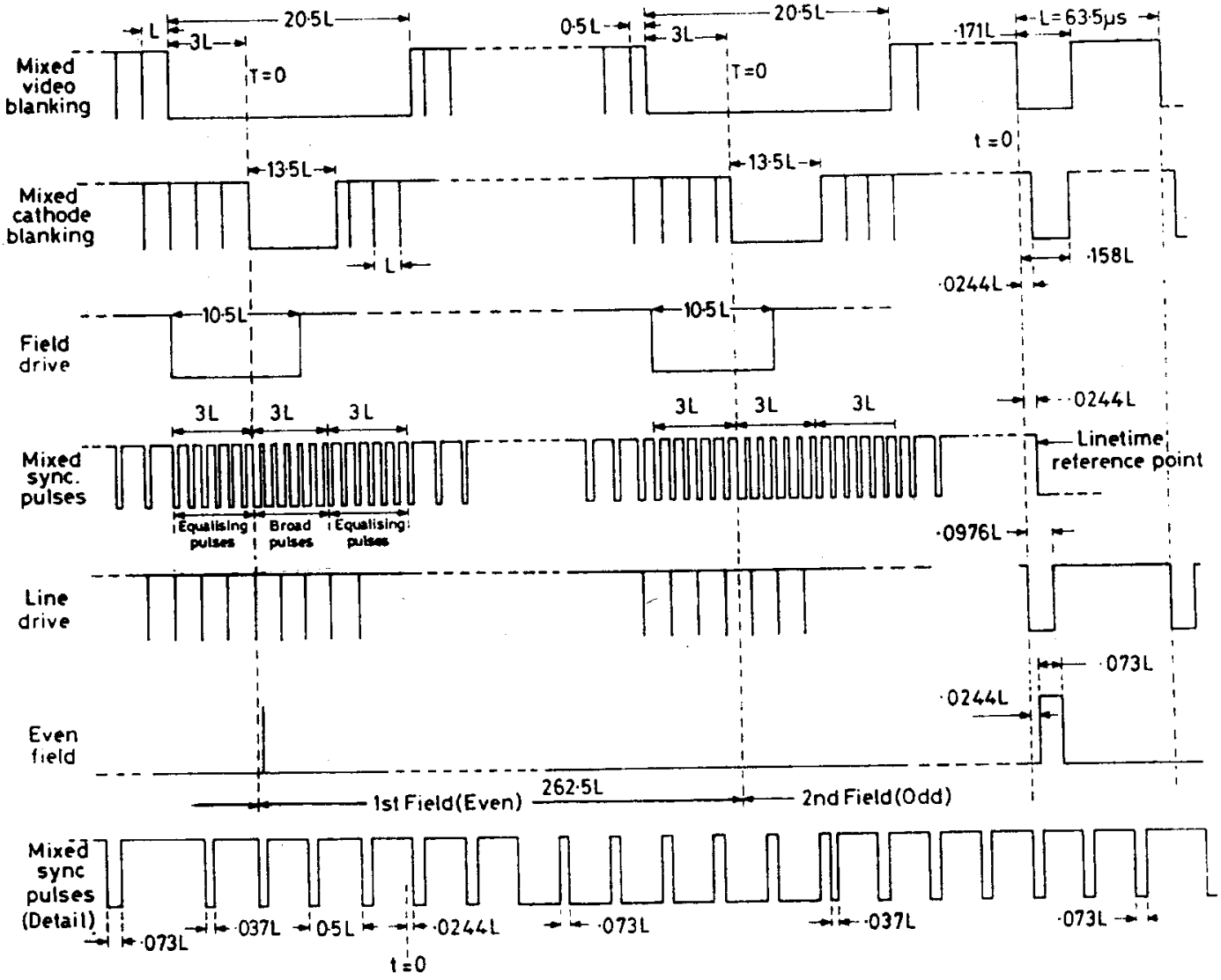
All outputs – mixed sync, mixed video blanking, line drive, reference clock, mixed cathode blanking, even field and field drive have internal 10kΩ pull-up resistors. Edge speeds and sourcing capability can be increased, if required, by the addition of external pull-up resistors. These should have a minimum value of 2kΩ.

OUTPUT WAVEFORMS

(a) 625 line CCIR standard output (Mode = 1).
Crystal frequency = 2.5625 MHz.
Line frequency = 15.625 kHz, Field frequency = 50 Hz.
Line period = 64 μs, Field period = 20 ms.



(b) 525 line EIA standard output (Mode = 0).
Crystal frequency = 2.5830 MHz
Line frequency = 15.750 kHz, Field frequency = 60 Hz
Line period = 63.5 μs, Field period = 16.66 ms.



APPLICATIONS INFORMATION

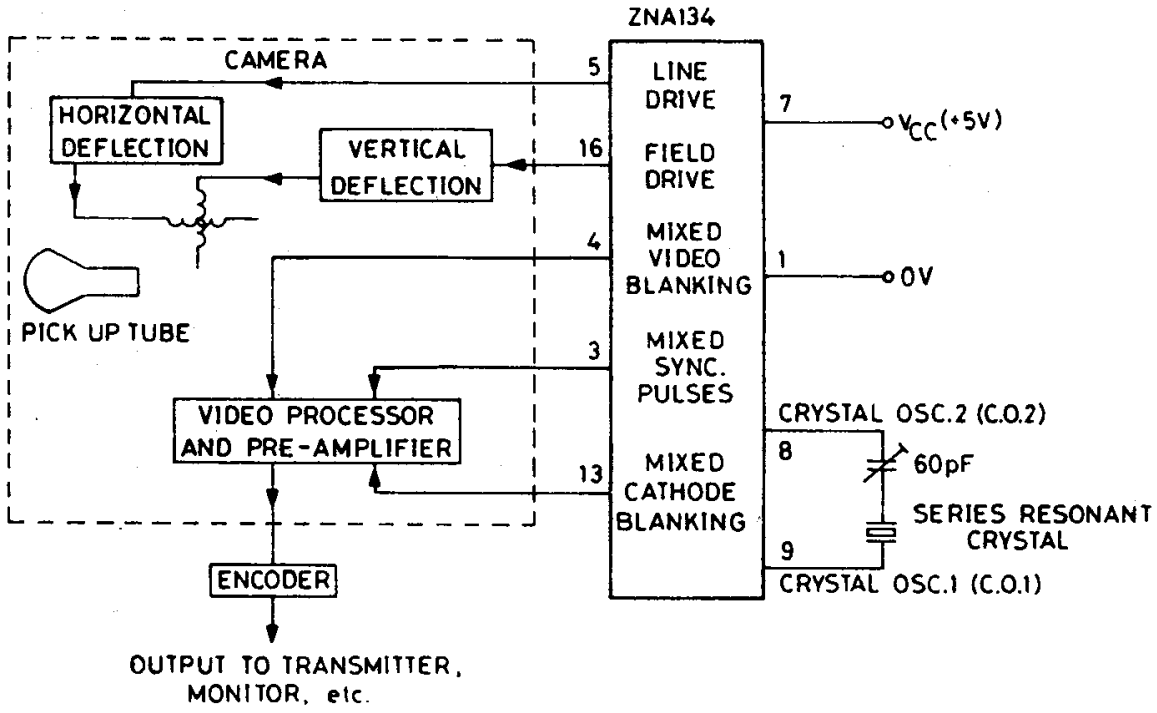


Fig. 1. Application in a TV system

The sync. pulse generator can be driven from an external oscillator if required. C.O.1 must then be connected via a 10kΩ resistor to V_{CC}. The external oscillator can then drive directly into C.O.2 input as shown in Fig. 2.

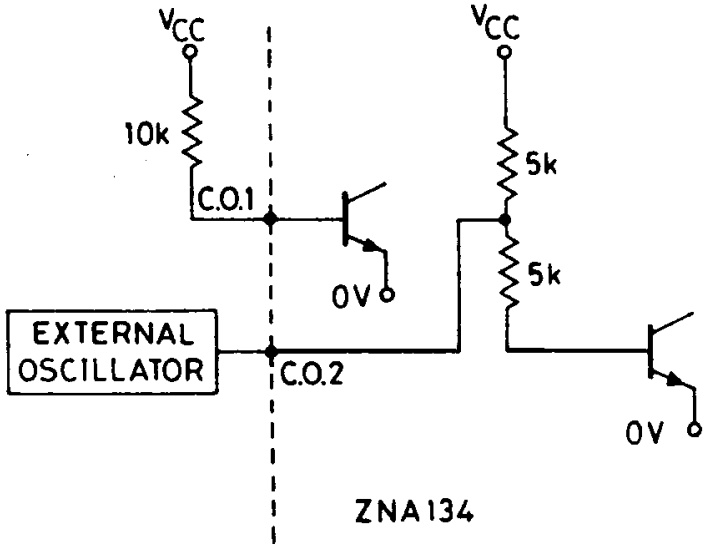


Fig. 2

Mode input (pin 2) can be connected directly to V_{CC} or 0V for 625 or 525 line operation respectively Any of the inputs: vertical reset, horizontal reset, line add, line subtract, not being used should be connected to 0V.

SIMPLE METHOD OF SYNCHRONISATION USING VERTICAL AND HORIZONTAL RESET

Line synchronisation (Fig. 3) is achieved by using a narrow positive going pulse derived from the negative going edge of the Line Drive output of the first generator to drive the Horizontal Reset inputs of the other generators. This monostable pulse, which should have a width of 200 ns ± 40 ns, resets the generators to the start of a line (t = 0). This results in the Line Drive waveforms of the driven generators being one reference clock period (≃800 ns) delayed from the first generator. The C.O.2 pins of the generators must be connected together.

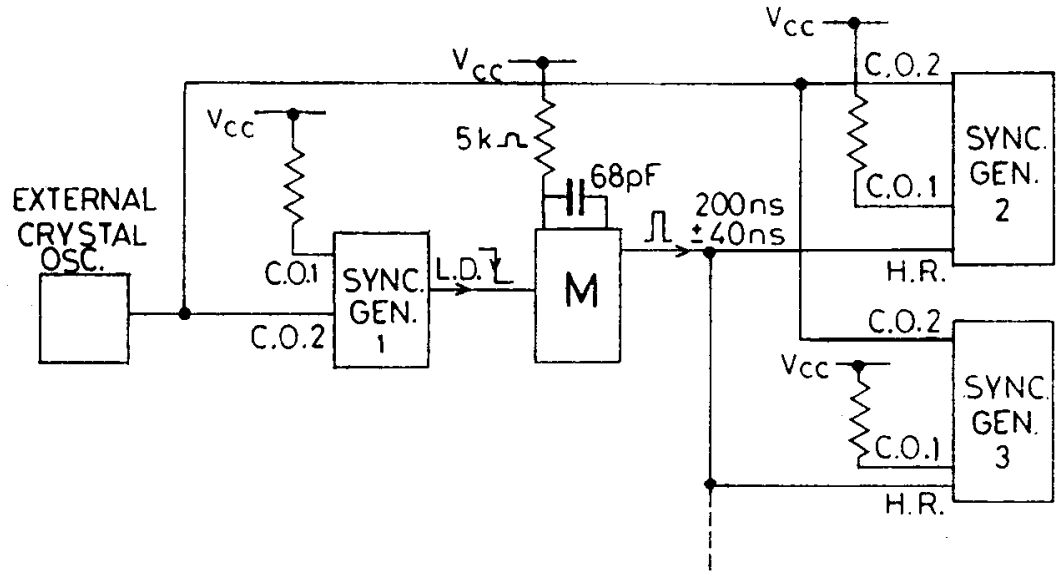


Fig. 3 Line Synchronisation using Horizontal Reset

Field Synchronisation (Fig. 4) is achieved by driving the Vertical Reset inputs of the driven generators directly from the Even Field output of the first generator (the Line drive outputs should already be in phase). This resets the generators to the start of the first field (T = 0, start of broad pulses.)

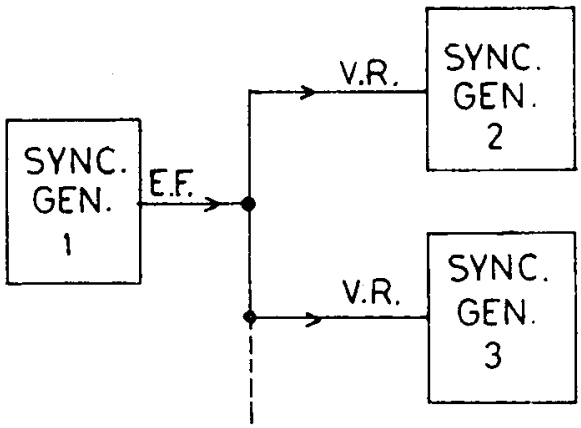


Fig. 4 Field Synchronisation using Vertical Reset

With this method of synchronisation, line sync and field sync are lost at the monitor for a brief period due to a sudden change in the Mixed Sync waveform. Hence it is only suitable for CCTV systems where momentary loss of picture is not critical or where the generators are to be synchronised automatically at power switch on.

SYNCHRONISATION USING THE LINE ADD/SUBTRACT FACILITY

This is suitable where generator lock must be achieved gradually, i.e. without loss of picture at the receiver, as in studio camera systems.

Line Synchronisation can be achieved smoothly by the use of a phase locked loop technique rather than the direct Horizontal Reset technique (Fig. 5).

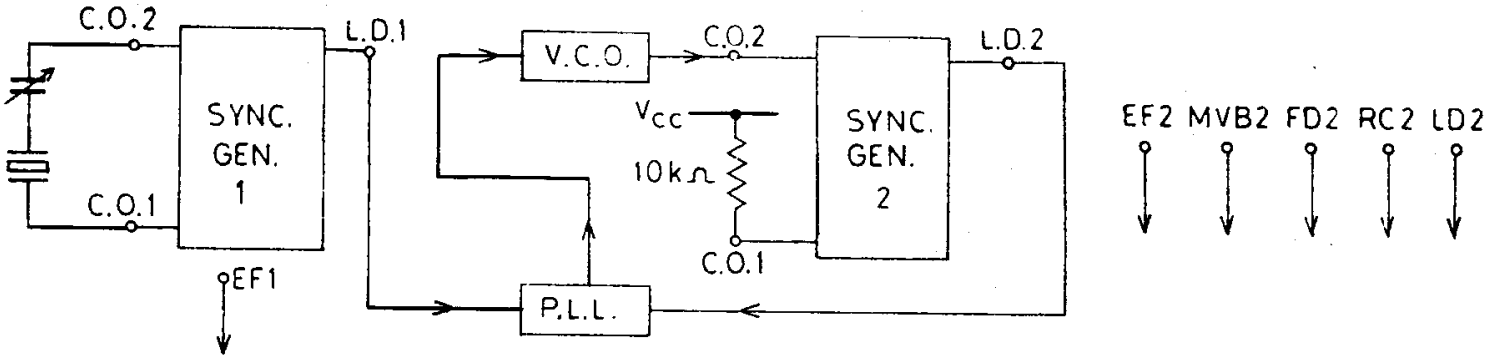


Fig. 5 Line Lock Circuitry

Field Synchronisation (Fig. 6). The generator waveforms are brought into synchronisation by adding or subtracting one line per frame to the second generator until the waveforms are exactly in phase. This is achieved by adding or inhibiting pulses at the start of the first full line after field blanking, thus preventing any changes to the mixed sync. waveform during the broad and equalising pulse periods. Lines are 'added' by clocking the vertical counter faster than the normal half line rate. Setting Line Add high for a period equal to 4 Reference Clock pulses, increments the vertical counter by one line thus effectively reducing the field period by one line.

Lines are 'subtracted' by inhibiting the clock pulses to the vertical counter. Setting Line Subtract high for a period of one line leaves the state of the vertical counter unchanged for one line thus effectively increasing the field period by one line.

Hence the add or subtract periods are generated by counting Reference Clock or Line Drive pulses respectively with a 3 bit counter.

Lines are added or subtracted until the generators are in phase. The two Even Field outputs together generate a pulse which inhibits the add/subtract circuitry when an in-phase condition occurs.

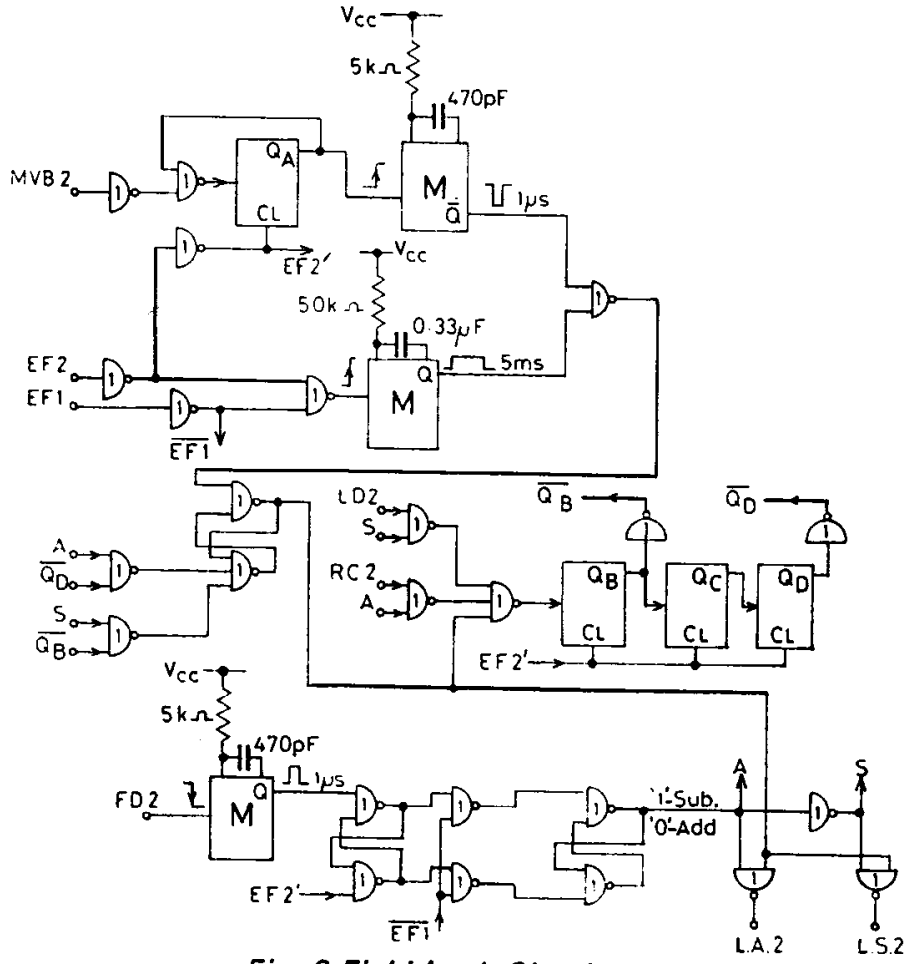


Fig. 6 Field Lock Circuitry

Lines are added to the second generator if EF2 is less than one field period delayed from EF1, and subtracted if EF2 is greater than one field period delayed from EF1 to reduce synchronisation time The add/subtract circuitry can be built using nine TTL packages:-

4 off	7402
1 off	7427
1 off	7404
1 off	74123
1 off	74121
1 off	7493

The circuit in Fig. 6 adds or subtracts one line per frame but this could be extended to two or more lines per frame by adding further bits to the 3 bit counter and decoding the relevant states. Similarly half a line per frame can be added by decoding 'QC' instead of 'QB'.

The circuit operates in 625 or 525 line mode without any changes to the component values.