National Semiconductor

APRIL 1978

INS8154 N-Channel 128-by-8 Bit RAM Input/Output (RAM I/O)

General Description

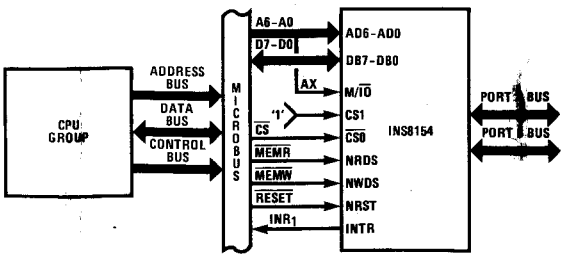
The RAM Input/Output Chip is an LSI device which provides random access memory and peripheral interfacing for microcomputer systems. The RAM portion contains 1024 bits of static RAM organized as 128x8. The I/O portion consists of two peripheral ports of eight bits each. Each of the I/O pins in the two ports may be defined as an input or an output to provide maximum flexibility. Each port may be read from or written to in a parallel (8-bit byte) mode. To improve efficiency and simplify programming in control-based applications, a single bit of I/O in either port may be set, cleared or read with a single microprocessor instruction. In addition to basic I/O, one of the ports, port A, may be programmed to operate in several types of strobed mode with handshake. Strobed mode together with optional interrupt operation permit both high speed parallel data transfers and interface to a wide variety of peripherals with no external logic.

The RAM I/O is an n-channel silicon gate device packaged in a 40-pin dual-in-line package. It operates with a single 5-volt power supply and is fully TTL compatible.

Features

- 128x8 RAM
- Single +5-volt power supply
- Low power dissipation
- Fully static operation
- Completely TTL compatible
- Two 8-bit programmable I/O ports
- I/O port A has TRI-STATE® capability
- Handshake controls for strobed mode of operation
- Single bit I/O operations with single instruction
- Reduces system package count
- Direct interface with SC/MP
- Independent operation of RAM and I/O
- MICROBUS™* Compatible

INS8154 MICROBUS™ Configuration



NOTE

The INTR signal becomes active only in the strobed mode when a data transaction has occurred.

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INS8154 N-Channel 128-by-8 Bit RAM Input/Output (RAM I/O)

Absolute Maximum Ratings*

Voltage at Any Pin	−0.5 V to +7.0 V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.

DC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5 V ± 5% unless otherwise specified.)

Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage		2.0		V_{CC}+0.5	V
V_{IL}	Logical "0" Input Voltage		−0.5		0.8	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −100 μA	2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 2.0 mA			0.4	V
I_{LI}	Input Load Current	V_{IN} = 0V to 5.25V			±10	μA
I_{LO}	Output Leakage Current	High Impedance State			±10	μA
I_{CCI}	Power Supply Current	All Outputs Open, T_A = 25°C, NRST ≤ 0.8V		45	60	mA

AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ± 5% unless otherwise specified — see Note 1.)

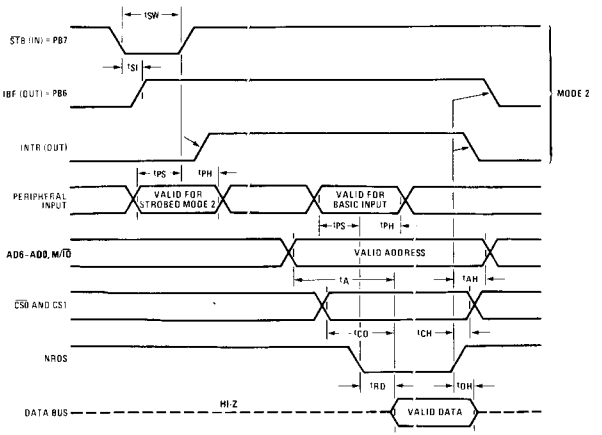
Parameter		Conditions	Min	Typ	Max	Units
READ CYCLE						
t_{SW}	$\overline{STB}$ Pulse Width (Mode 2 Only)		300			ns
t_{SI}	$\overline{STB}$ ↓ to IBF ↑ Delay (Mode 2 Only)				250	ns
t_{PS}	Peripheral Setup		50			ns
t_{PH}	Peripheral Hold		120			ns
t_{AH}	Address Hold		50			ns
t_{CH}	CS Hold		50			ns
t_{RD}	NRDS ↓ to Data Valid				350	ns
t_A	Access				560	ns
t_{CO}	Chip Select to Output				520	ns
t_{OH}	Data Valid After NRDS ↑		0	125		ns
	Output Load Capacitance				75	pF
WRITE CYCLE						
t_{WC}	Write Cycle (for RAM)		700			ns
t_{AS}	Address Setup		50			ns
t_{AH}	Address Hold		0			ns
t_{CS}	CS Setup		50			ns
t_{CH}	CS Hold		0			ns
t_{DS}	Data Setup		50			ns
t_{DH}	Data Hold		50			ns

AC Electrical Characteristics (cont'd)

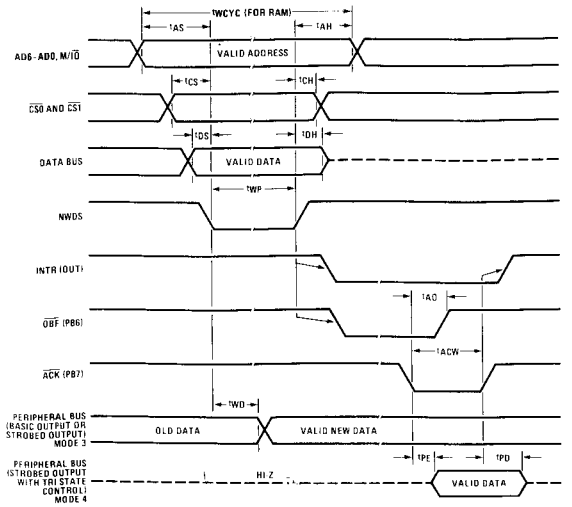
Parameter		Conditions	Min	Typ	Max	Units
WRITE CYCLE						
t_{WP}	NWDS Pulse Width		300			ns
t_{AO}	$\overline{ACK}$ ↓ to $\overline{OBF}$ ↑ (Modes 3 & 4 Only)				250	ns
t_{ACW}	$\overline{ACK}$ Pulse Width (Modes 3 & 4 Only)		300			ns
t_{WD}	Port Data Valid After NWDS ↓				300	ns
t_{PE}	$\overline{ACK}$ ↓ to Valid Output (Mode 4 Only)				300	ns
t_{PD}	$\overline{ACK}$ ↑ to Hi-Z (Mode 4 Only)		0	125		ns
	Output Load Capacitance				75	pF
t_{WRST}	Master Reset Pulse Width		300			ns

Note 1: All times measured from a valid logic "0" level = 0.8 V or a valid logic "1" level = 2.0 V.

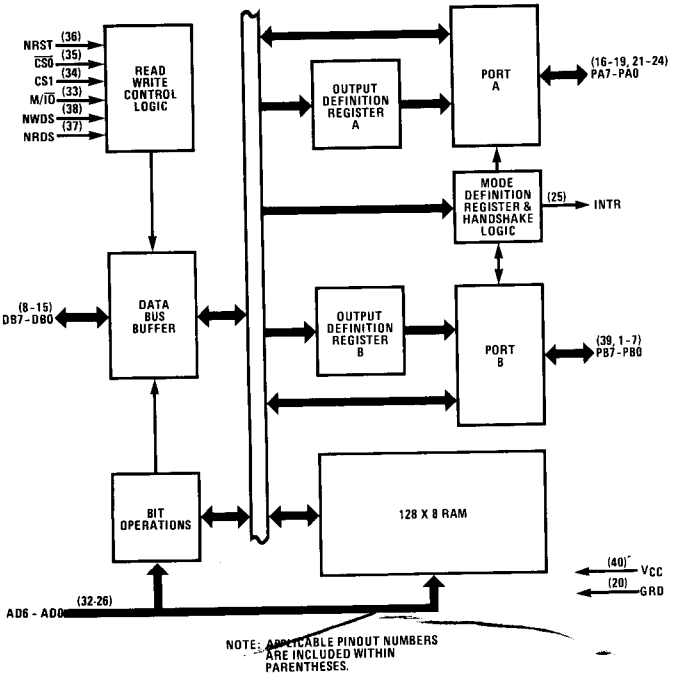
Read Cycle



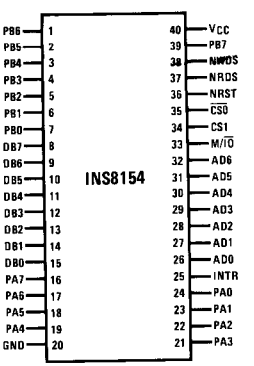
Write Cycle



INS8154 Block Diagram



Pin Configuration



Pin Names

DB7 - DB0	DATA BUS
AD6 - AD0	ADDRESS INPUT
NRST	RESET INPUT
M/IO	MEMORY/IO SELECT
CS0, CS1	CHIP SELECTS
NWDS	WRITE STROBE
NRDS	READ STROBE
PA7 - PA0	PORT A
PB7 - PB0	PORT B
INTR	INTERRUPT REQUEST
VCC	+5 VOLTS
GND	0 VOLTS

Basic Functional Description

The RAM I/O performs two separate but important functions in microcomputer systems. The first is data storage provided by the 128 x 8 RAM. The second function is peripheral interfacing provided by the two 8-bit I/O ports. The ability to program the configuration and operating modes of the I/O ports allows interfacing a microcomputer to a wide varity of peripherals with minimum external logic. Major functional blocks of the chip are shown in the block diagram; an operational summary of the chip is provided in figure 1. A description of the chip pinouts and a summary of the internal chip registers is given below.

(DB7 - DB0) Data Bus Buffers

The data bus buffer is a TRI-STATE, bidirectional, 8-bit buffer that is used to interface the RAM I/O to a microcomputer data bus. Data, control, and status information is transmitted to and received from the RAM I/O via the data bus buffers. Execution of a STORE instruction by the microprocessor may be used to transmit data and control information from the CPU to the RAM I/O. Execution of a LOAD instruction may be used to transmit data and status information from the RAM I/O to the CPU.

($\overline{CS0}$ and CS1) Chip Select Inputs

The combination of a low on $\overline{CS0}$ and a high on CS1 input pins enables communication between the RAM I/O and the microprocessor.

(M/$\overline{IO}$) Memory $\overline{I/O}$ Select

The state of the M/$\overline{IO}$ input pin determines whether communication between the CPU and RAM I/O chip will involve the RAM portion of the RAM I/O or the I/O portion. A high on M/$\overline{IO}$ selects the RAM while a low selects the I/O.

(NRDS) Read Strobe

NRDS is an active-low read strobe. A low on this pin enables data or status information to be read from the RAM I/O.

(NWDS) Write Strobe

NWDS is an active-low write strobe. A low on this pin enables data or control information to be written into the RAM I/O.

(AD6 - AD0) Address Inputs

The address input bus determines where in the RAM I/O communication will take place. When the RAM is selected, the address bus determines which of the 128 bytes of RAM will be read from or written into. When I/O is selected, the address determines which I/O or control register will be enabled for communication with the CPU. These pins are normally connected to the seven low address lines of the microprocessor.

RAM

The RAM contained on the RAM I/O chip consists of 1024 bits organized as 128 eight-bit bytes. Since the RAM is fully static, no refresh or clocks are required. Data out of the RAM is of the same polarity as data in, and readout is nondestructive. The RAM is a standard six-transistor cell similar in design to the 2102A static RAM.

(MDR) Mode Definition Register

The Mode Definition Register is an internal control register that determines the operating mode of port A. This register is *write only*. If a read operation is performed with the address set to that of the MDR, the data bus will remain in the high impedance state.

(PA7 - PA0, PB7 - PB0) Peripheral Ports A and B

The RAM I/O contains two eight bit I/O ports: port A and port B. Each port consists of an eight-bit output data latch with buffer and an eight-bit input data latch. Full flexibility is provided with the ability to define any bit of the two ports either as an input or as an output. Bit set, clear and read of all I/O pins are also provided. Moreover, port A may be operated in strobed input or strobed output modes.

Output Definition Registers — ODRA and ODRB

Associated with each port is an output definition register (ODR). Each ODR is an eight-bit latch that defines which of the I/O pins in the respective port are to be used as outputs. ODRA controls the direction of port A and ODRB controls the direction of port B. Both ODRs are *write only* registers. If a read operation is performed with the address set to that of an ODR, the data bus will remain in the high impedance state.

(INTR) Interrupt Request

The interrupt request (INTR) output is an active high signal used to interrupt the microprocessor when a strobed mode data transaction has occured. This signal is active only when port A is in the strobed mode. INTR will be set to a low when a master reset is applied (NRST set low).

(NRST) Master Reset

NRST is the master reset input for the RAM I/O chip. A low on this pin clears all registers in the I/O portion of the chip (MDR, ODRA, ODRB, and the port output data latches) and places the data bus in the high impedance state independent of any other control strobes. After a master reset, the I/O ports will both be in the basic I/O mode and configured as inputs. The master reset does not change any data previously stored in the RAM and does not allow data to be written into or read from the RAM while NRST is low.

Operation	NRST	NRDS	NWDS	$\overline{CS0}$	CS1	M/$\overline{IO}$	A6	A5	A4	A3	A2	A1	A0
RAM OPERATIONS													
Data Bus → RAM	1	1	0	0	1	1	X	X	X	X	X	X	X
RAM → Data Bus	1	0	1	0	1	1	X	X	X	X	X	X	X
BIT OPERATIONS													
Set Bit Port A	1	1	0	0	1	0	0	0	1	0	B2	B1	B0
Clear Bit Port A	1	1	0	0	1	0	0	0	0	0	B2	B1	B0
Read Bit Port A	1	0	1	0	1	0	0	0	X	0	B2	B1	B0
Set Bit Port B	1	1	0	0	1	0	0	0	1	1	B2	B1	B0
Clear Bit Port B	1	1	0	0	1	0	0	0	0	1	B2	B1	B0
Read Bit Port B	1	0	1	0	1	0	0	0	X	1	B2	B1	B0
PORT OPERATIONS													
Port A → Data Bus	1	0	1	0	1	0	0	1	0	0	0	0	0
Data Bus → Port A	1	1	0	0	1	0	0	1	0	0	0	0	0
Port B → Data Bus	1	0	1	0	1	0	0	1	0	0	0	0	1
Data Bus → Port B	1	1	0	0	1	0	0	1	0	0	0	0	1
CONTROL OPERATIONS													
Data Bus → Output Definition A	1	1	0	0	1	0	0	1	0	0	0	1	0
Data Bus → Output Definition B	1	1	0	0	1	0	0	1	0	0	0	1	1
Data Bus → Mode Definition Register	1	1	0	0	1	0	0	1	0	0	1	0	0
DISABLE FUNCTION													
Master Reset	0	X	X	X	X	X	X	X	X	X	X	X	X
Data Bus → Hi-Z	1	1	1	0	1	X	X	X	X	X	X	X	X
Data Bus → Hi-Z	1	X	X	1	X	X	X	X	X	X	X	X	X
Data Bus → Hi-Z	1	X	X	X	0	X	X	X	X	X	X	X	X

Figure 1. Truth Table

Detailed Operation

RAM

The internal organization of the RAM and a typical RAM memory cell are shown in figure 2; the 1024-bit memory is structured in a 32-column by 32-row matrix. The proper row is selected by the five higher-order address (AD6-AD2) inputs; the 8-bit byte in this row is selected by eight 1-of-4 column decoders controlled by the two lower-order address (AD1-AD0) inputs. A timing diagram of RAM read/write operations is shown in figure 3. While RAM cannot be read from or written into during a master reset (NRST), the reset signal does not affect the data in RAM.

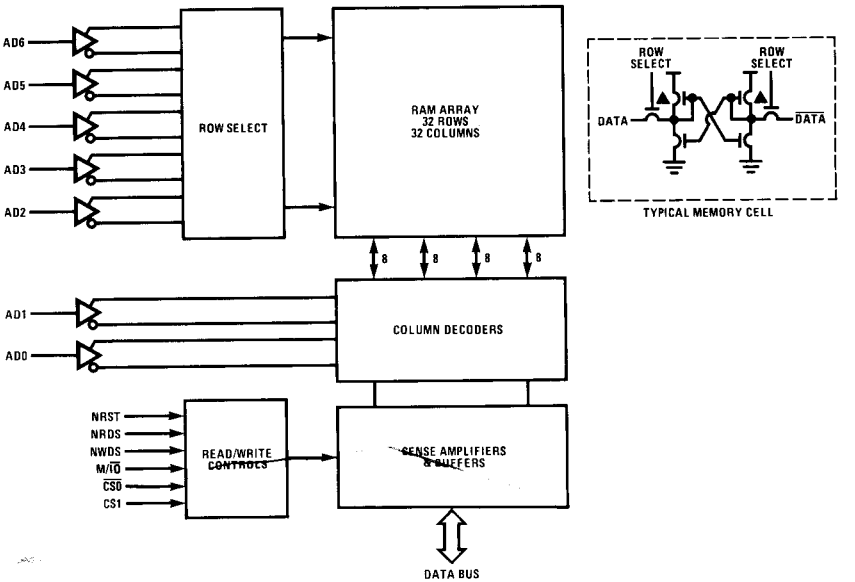
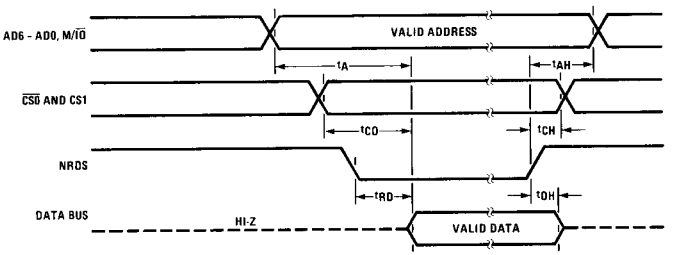


Figure 2. RAM Organization

RAM Read Operation



RAM Write Operation

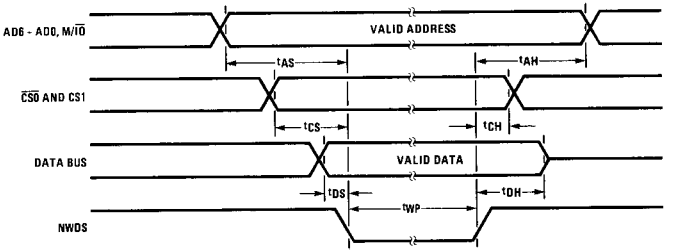


Figure 3. RAM Read/Write Timing

Mode Definition Register

The mode definition register defines the operating mode for port A. Port B is always in the basic I/O mode. There are four operating modes for port A:

Mode 1 – basic I/O

Mode2 – strobed input

Mode 3 – strobed output

Mode 4 – strobed output with TRI-STATE control

In mode 1, basic I/O, there is no handshaking and data is simply written to or read from the specified port. Port B is always in this mode. When NRST goes low, both port A and port B are set to the basic I/O mode with all bits set to input. Mode 2, strobed input, provides a means for transferring data from the peripheral into port A in response to handshake or strobe signals. Mode 3, strobed output, provides a means for transferring data from port A to the peripheral in response to strobes or handshake signals. Mode 4, strobed output with TRI-STATE control is similar to mode 3 except that port A is in the high impedance state until the handshake signal goes active. Figure 4 summarizes what data should be written into the MDR to place port A in the desired mode. When port A is operated in any one of the three strobed modes, two pins of port B are used for handshake control functions; accordingly, only six of the eight port B pins are available for data input/output bits.

Output Definition Registers

Although addressed separately from the ports, the output definition registers are an integral part of the I/O ports as shown in figure 5. This figure shows the input data latch and output data latch/buffer of a bit in a port and the bit of the ODR associated with it. Thus there is one bit of an ODR associated with each peripheral I/O pin in port A and port B. If a low or "0" is written into the ODR, the output data buffer associated with it will be disabled, and the I/O bit is in the input mode. If a high or "1" is written into the ODR, the I/O bit is in the output mode. When strobed mode operation (modes 2 through 4) is defined for port A via the MDR, it is also necessary to set up proper input/output definition in ODRA for port A.

Basic I/O – Mode 1

In the basic I/O mode of operation data is simply written to or read from a port without handshake signals; the interrupt request (INTR) is always low when port A is operated in this mode. Port B is always in the basic I/O mode, whereas the MDR bit 5 (M in figure 4) must be set to zero to define port A in the basic I/O mode. Since the MDR, ODRA and ODRB are all cleared by a master reset, both port A and port B will be in the basic input mode after a master reset (NRST set low).

Figure 6 shows a timing diagram for basic output. When the microprocessor performs a write operation to a port, the data on the data bus is latched in the output latch on the leading edge of the write strobe. The data will remain valid until another write to the port with new data occurs. If the new data written is the same as the old data, then no change will occur so long as the proper data and strobe timing is maintained.

Figure 7 shows a timing diagram for basic input. When the microprocessor reads the port, the peripheral data is *latched* in the input latch on the leading edge of the read strobe. The data bus buffers are enabled so the contents of the latch are gated on to the system data bus. The data remains latched until the end of the read cycle (i.e., until the trailing edge of the read strobe). Latching the input data in this manner allows the chip to synchronize asynchronous peripheral signals with slow rise and fall times to the microprocessor.

A port can have some input pins and some output pins, since there is an ODR latch for each bit in the port. A write to a pin defined as an input will load a new value into the output data latch, but since the output data buffer is disabled, it will have no effect on the I/O pin. A data read from I/O pins defined as outputs will read the data from the output data latch. The data will be read properly only if the I/O lines are permitted to be greater than V_{IH} for a logic 1 output and less than V_{IL} for a logic 0 output. If the I/O pins are loaded in such a way that valid levels are not reached, the data read will not always agree with the data stored in the output data latch.

Bit Set, Clear and Read

In addition to reading and writing each port as an eight-bit parallel byte, it is also possible to set, clear or read any individual bit in either port. Bit set or clear is performed by doing a write operation with the chip selected and the proper address. Since the address determines which bit is operated on and whether it is set or cleared, the eight data bus lines are all don't-care for a bit set or clear. This permits the microprocessor to do a bit set or clear with a single instruction without initially setting up the accumulator. The three low order bits of the address determine which bit of the port is set or cleared (e.g., AD2 = 0, AD1 = 1 and AD0 = 0 would indicate bit 2). Address bit 3 (AD3) determines if port A or port B is acted upon. Address bit 4 (AD4) determines if the operation is a bit set or clear.

When a bit read is performed, the selected bit is placed on data bus bit 7 (DB7) and all other bits of the data bus are set to zero. The bit is selected by reading from the chip with the same addresses described for bit set and clear. All bit operations are summarized in figure 8.

Besides simplifying programming in control applications, bit operations are used to control interrupt enable when port A is in the strobed mode. The timing for bit operations is the same as that for basic input/output except that, for bit set and bit clear operations, the data bus is a "don't care." A bit set to a pin whose previous value was a "1" or a bit clear to a pin whose previous value was a "0" will not cause that pin to leave its previous value, even momentarily.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Bit Location
TS	OUT	M	–	–	–	–	–	MDR Bit Name
X	X	0	X	X	X	X	X	Basic I/O
X	0	1	X	X	X	X	X	Strobed Input
0	1	1	X	X	X	X	X	Strobed Output
1	1	1	X	X	X	X	X	Strobed Output with TRI-STATE Control

Figure 4. Mode Definition of Port A with MDR

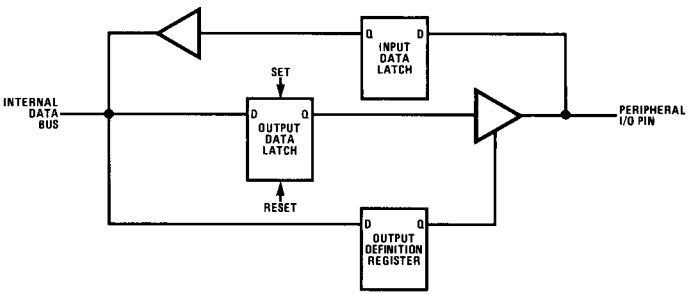


Figure 5. Internal Logic of One Bit of an I/O Port with ODR

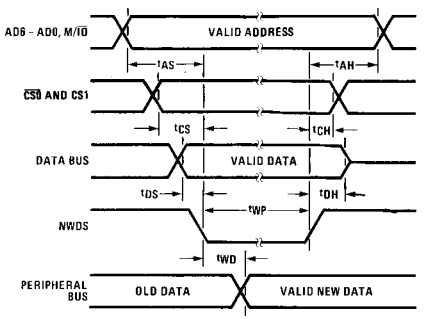


Figure 6. Basic Output Timing

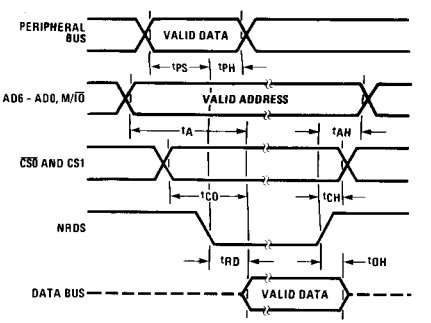


Figure 7. Basic Input Timing

	NRDS	NWDS	A4	A3	A2	A1	A0
BIT SET & CLEAR							
Bit Set, Port A	1	0	1	0	B2	B1	B0
Bit Clear, Port A	1	0	0	0	B2	B1	B0
Bit Set, Port B	1	0	1	1	B2	B1	B0
Bit Clear, Port B	1	0	0	1	B2	B1	B0
BIT READ Selected Bit → DB7 0 → DB6 - DB0							
Bit Read, Port A	0	1	X	0	B2	B1	B0
Bit Read, Port B	0	1	X	1	B2	B1	B0

Bit Operations Enabled When $\overline{CS0}$ = 0, CS1 = 1, M/$\overline{IO}$ = 0, A6 = 0, & A5 = 0

B2, B1, & B0 select which bit is selected (B0 is least significant bit).

Figure 8. Bit Operations

Strobed Input (Port A) – Mode 2

This mode allows data to be read from a peripheral in a two-step transaction. First, the peripheral strobes data into the RAM I/O input latch and notifies the microprocessor that data is ready to be read. Second, the processor reads the contents of the RAM I/O input latch and resets the handshake control signals for the next transaction to take place. Transferring data in two steps frees the microprocessor to undertake other tasks in between data transfers from the port A peripheral. Figure 9 shows the signal timing and figure 10 shows a logic diagram for the handshake signals. The handshake control signals are as follows:

$\overline{STB}$ ($\overline{Strobe}$)

The $\overline{STB}$ signal is an active-low strobe generated by a peripheral to signify that data is valid at the peripheral bus on the trailing edge of this strobe. This signal is fed into pin PB7 of the RAM I/O. $\overline{STB}$ latches peripheral bus data into the RAM I/O input data latch on its trailing edge. This does *not* require the RAM I/O to be selected. Should $\overline{STB}$ pulse low more than once before the arrival of NRDS, the data stored in the RAM I/O input data latch will be the *last* stored data.

IBF (Input Buffer Full)

The IBF signal is an output from the RAM I/O driven by pin PB6; IBF is set by the leading edge of $\overline{STB}$ and is reset by the trailing edge of NRDS when the microprocessor is performing a byte-read from port A. IBF high tells the peripheral that data is latched in the port A input data latch. IBF goes low on the trailing edge of the microprocessor NRDS strobe to notify the peripheral that data has been read in the microprocessor and that the next transaction can now take place. The microprocessor can override IBF by doing a bit set or bit clear to PB6.

IE (Interrupt Enable)

IE is the output data latch of PB7, whose output is ANDed with the interrupt request latch to produce the INTR signal. IE is zero after a master reset (NRST) but may be written into from the microprocessor by doing a bit set/clear to PB7.

INTR (Interrupt Request)

When enabled by IE, INTR is an output that is set on the trailing edge of $\overline{STB}$, requesting the microprocessor to read the data in the port A input data latch. When the microprocessor responds to read port A, the trailing edge of NRDS resets INTR. Should IE *not* be set, INTR will remain low.

In a multiple-interrupt application, the microprocessor can poll the RAM I/O for the existence of an interrupt request by doing a bit read of PB7. Being able to read the INTR status on the microprocessor system bus is useful in multi-interrupt schemes to find the originator of an interrupt.

Parallel write operations to port B while port A is in any one of its strobed modes will leave bits PB6 and PB7 unaffected. Thus, port B now has 6 data I/O bits associated with it and the handshake bits PB6 and PB7 respond only to valid changes in handshake status or to bit set/bit clear operations.

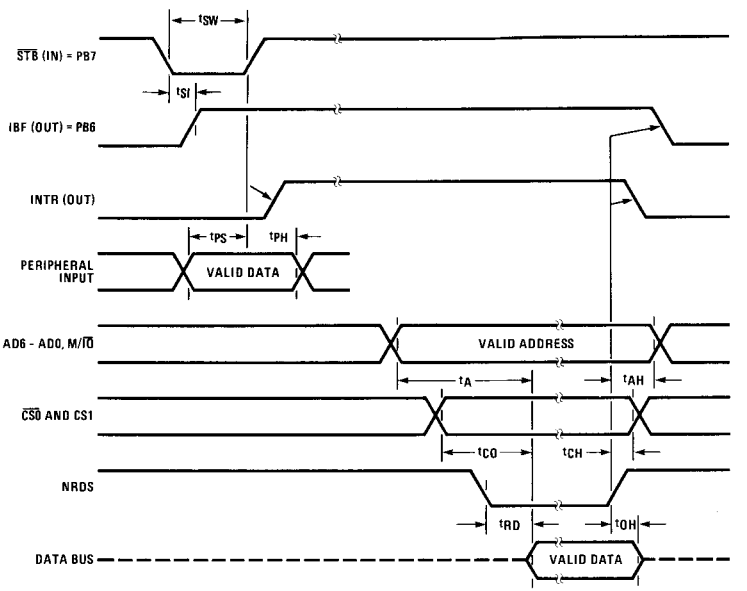
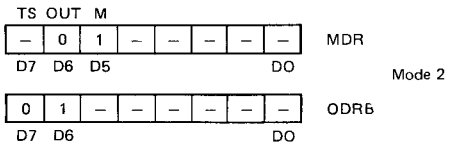


Figure 9. Strobed Input, Mode 2 Timing

Initializing Strobed Input – Mode 2

Prior to operation, an initialization procedure must be undertaken. The MDR must have a "1" written into bit 5 and a "0" written into bit 6. The ODRA must have "0s" written into it to identify the pins in port A which will function in mode 2. The ODRB must have a "0" written into PB7 in order to make it an input which will receive $\overline{STB}$ from the peripheral. Also, PB6 must be defined as an output so that it can drive the IBF signal. The remaining six lower bits of ODRB are configured as needed for the basic input/output transactions occuring in port B.



ODRA = "0s" at mode 2 pins.

Writing to the MDR to define mode 2 operation will automatically initialize both IBF and INTR in such a manner that they will be expecting the peripheral to begin the first I/O transaction with a $\overline{STB}$ strobe, i.e., both INTR and IBF will initialize low when the above write to the MDR takes place.

Handshake Status

Handshake status control signals IBF and INTR will be reset by a microprocessor LOAD instruction only if it is addressed to port A as a byte read. A parallel write or bit write or bit read to port A will *not* affect handshake status. A byte read or write to port B will not affect handshake status either, since PB6 and PB7 are masked from byte writes to port B when port A is in any of its strobed modes. It is possible, however, to override IBF or IE by an appropriate bit write to PB6 or PB7, respectively.

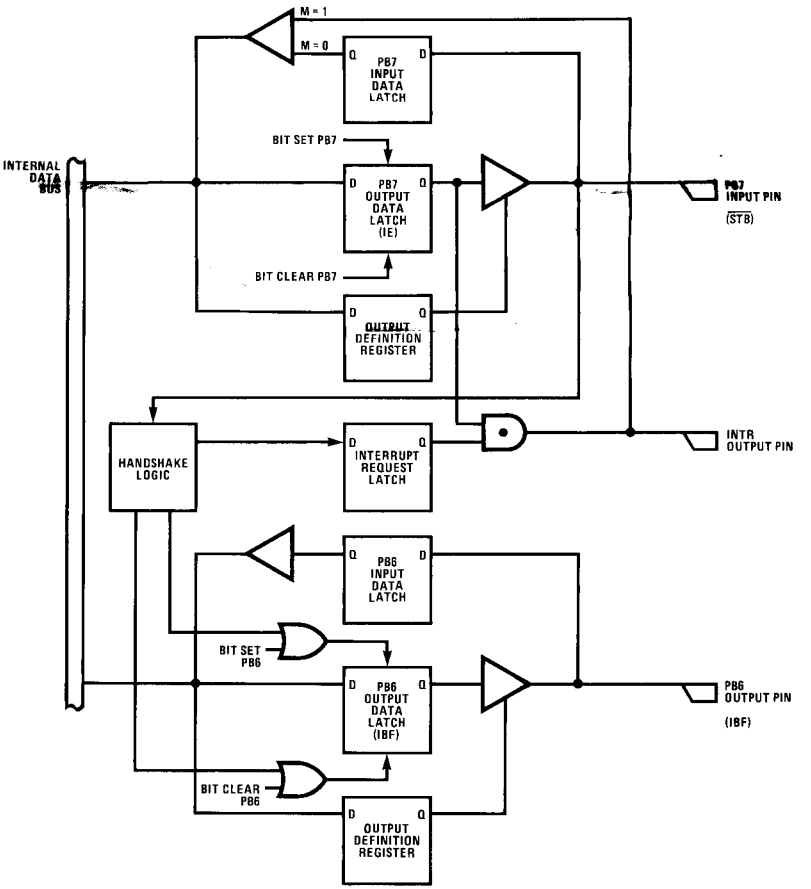


Figure 10. Strobed Input, Mode 2 Handshake Logic

Strobed Output (Port A) – Mode 3

This mode allows outputting data from the CPU to an asynchronous peripheral. The CPU writes into the output latch of the RAM I/O; in turn this creates a handshake signal which notifies the peripheral that its bus has new data on it. The peripheral reads the port A bus and returns the handshake signals to their previous state, awaiting the next CPU write. The peripheral bus is always being driven by the port A buffers in this mode. Pertinent timing relationships are shown in figure 11 and a logic diagram showing the handshake signals is shown in figure 12.

The handshake signals associated with mode 3 are the following:

$\overline{\text{ACK}}$ ($\overline{\text{Acknowledge}}$)

$\overline{\text{ACK}}$ is an active-low strobe generated by peripheral to read the data present on its bus. $\overline{\text{ACK}}$ drives the RAM I/O PB7 input and it sets the $\overline{\text{OBF}}$ signal on its leading edge and sets the INTR on its trailing edge; for this to happen, the RAM I/O need not be selected.

$\overline{\text{OBF}}$ ($\overline{\text{Output Buffer Full}}$)

$\overline{\text{OBF}}$ is an active-low signal generated by RAM I/O PB6 output. $\overline{\text{OBF}}$ goes low in response to the trailing edge of NWDS for a parallel write to port A and returns high on the leading edge of $\overline{\text{ACK}}$. $\overline{\text{OBF}}$ being low signals to the peripheral that valid data is now ready to be read on the peripheral bus.

IE (Interrupt Enable)

This is the same as for mode 2.

INTR (Interrupt Request)

When enabled by IE, INTR is set on the trailing edge of $\overline{\text{ACK}}$ and reset on the trailing edge of NWDS when a byte write to port A occurs.

The value of INTR can be read from the CPU data bus side by means of a bit read to PB7. This is useful in locating the originator of an interrupt in a multi-interrupt scheme.

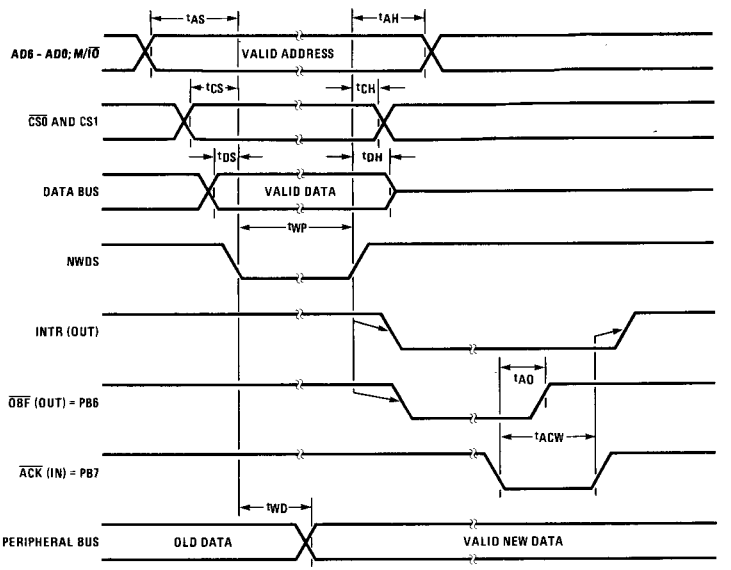
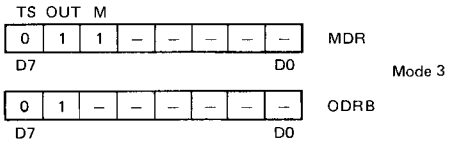


Figure 11. Strobed Output, Mode 3 Timing

Initializing Strobed Output — Mode 3

To initialize for mode 3 operation, the MDR must have "1s" written into bits 5 and 6. A "0" must also be written into bit 7.

The ODRA must have "1s" written into it to identify the bits of port A which will function in mode 3. The ODRB must have a "0" in PB7 in order to make it an input which will receive $\overline{ACK}$ from the peripheral. Also, PB6 must be defined as an output so that it can drive the $\overline{OBF}$ signal. The remaining 6 lower order bits of port B are configured as needed for the basic I/O transactions occurring in port B.



ODRA = "1s" at mode 3 pins.

Writing to the MDR to define mode 3 operation will automatically initialize both $\overline{OBF}$ and INTR such that the RAM I/O will be expecting the first strobed operation to take place. Both INTR and $\overline{OBF}$ are initialized high for mode 3, provided IE is set to a "1." If IE is set to "0," INTR will not initialize high.

Handshake Status — Mode 3

Handshake status control signals $\overline{OBF}$ and INTR will be reset low by a CPU STORE instruction only if it is addressed to port A as a *parallel write.* A parallel read or any bit operation to port A will *not* affect handshake status. A word read or write to port B will not affect handshake status either, since PB6 and PB7 are masked from word writes to port B when port A is in any of its strobed modes. It is possible, however, to override $\overline{OBF}$ or IE by an appropriate bit write to PB6 or PB7, respectively.

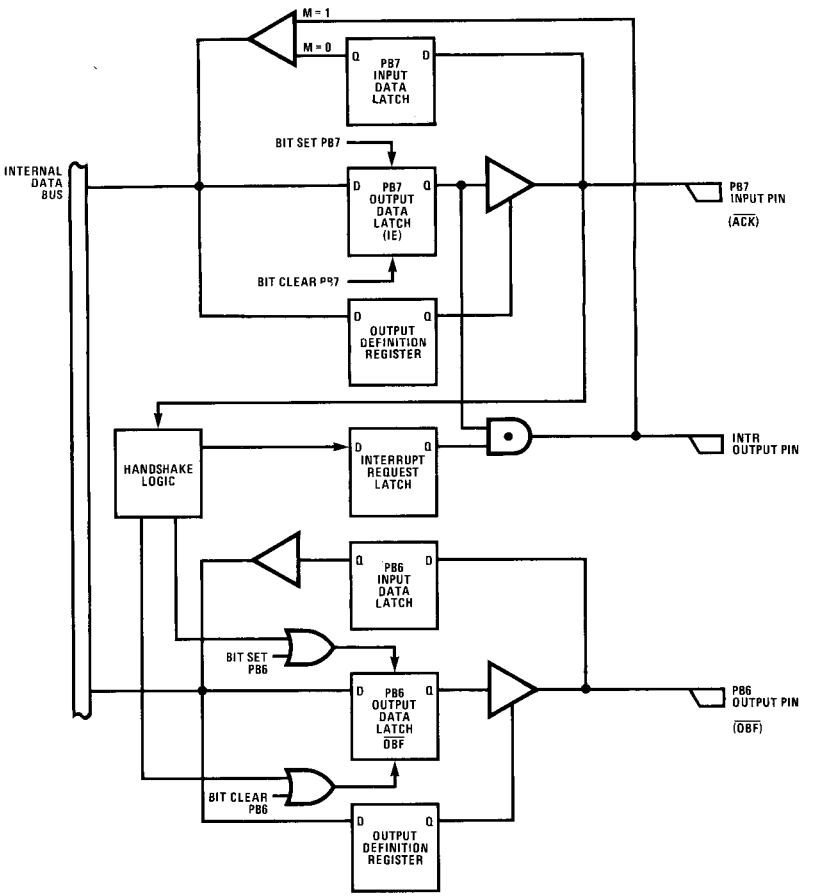


Figure 12. Strobed Output, Mode 3 Handshake Logic

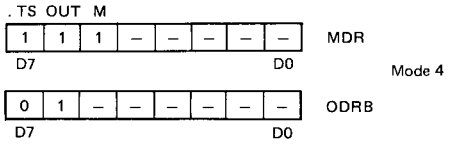
Strobed Output with TRI-STATE Control — Mode 4

This mode is similar to mode 3 in that it uses the same handshake signals and transfers data in the same direction. A timing diagram for mode 4 is shown in figure 13. Handshake logic is shown in figure 12. The main difference from mode 3 is the fact that the peripheral bus is in the TRI-STATE condition at all times except when $\overline{ACK}$ is low, enabling the RAM I/O to drive the peripheral bus to its valid state.

The CPU writes into the output latch of the RAM I/O; this resets INTR and $\overline{OBF}$ but the peripheral bus remains in TRI-STATE until the peripheral responds with a low-going $\overline{ACK}$ strobe. The $\overline{ACK}$ strobe enables the RAM I/O port output buffers to drive the peripheral bus active during this strobe time. The leading edge of $\overline{ACK}$ sets the $\overline{OBF}$ and the trailing edge of $\overline{ACK}$ sets INTR. The trailing edge of NWDS for a byte write to port A resets both $\overline{OBF}$ and INTR the same as in mode 3.

Initializing Strobed Output — Mode 4

To initialize for mode 4 operation, the MDR must have "1s" written into bits 5, 6, and 7. The ODRA must have "1s" written into it to identify the bits of port A which will function in mode 4. The ODRB must have a "0" in bit 7 and a "1" in bit 6.



ODRA = "1s" at mode 4 pins.

Writing to the MDR to define mode 4 operation will automatically initialize both $\overline{OBF}$ and INTR high such that the RAM I/O will be expecting the first strobed operation to take place, provided IE is set to a "1." If not, INTR will not be initialized high.

Handshake Status — Mode 4

Handshake status control signals $\overline{OBF}$ and INTR will be reset low by a CPU STORE instruction only if it is addressed to port A as a parallel write. A parallel read or any bit operation to port A will *not* affect handshake status. A word read or write to port B will not affect handshake status either, since PB6 and PB7 are masked from word writes to port B when port A is in any of its strobed modes. It is possible, however, to override $\overline{OBF}$ or IE by an appropriate bit write to PB6 or PB7, respectively.

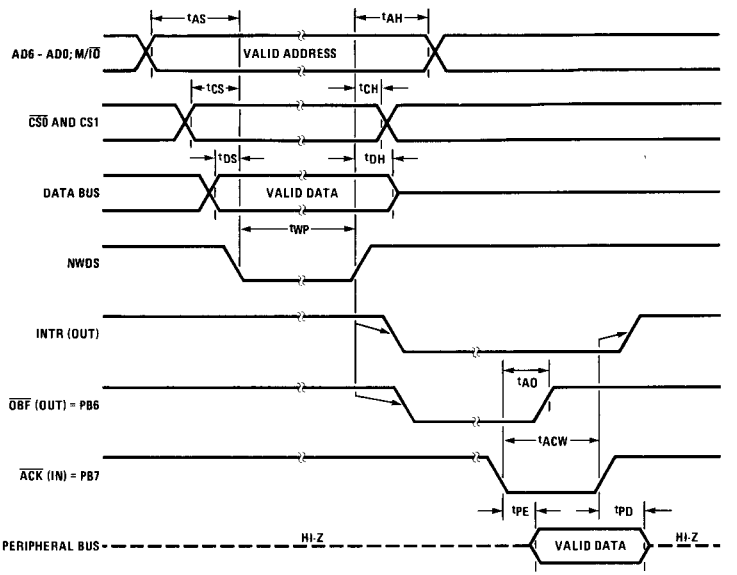


Figure 13. Strobed Output with TRI-STATE Mode 4 Timing

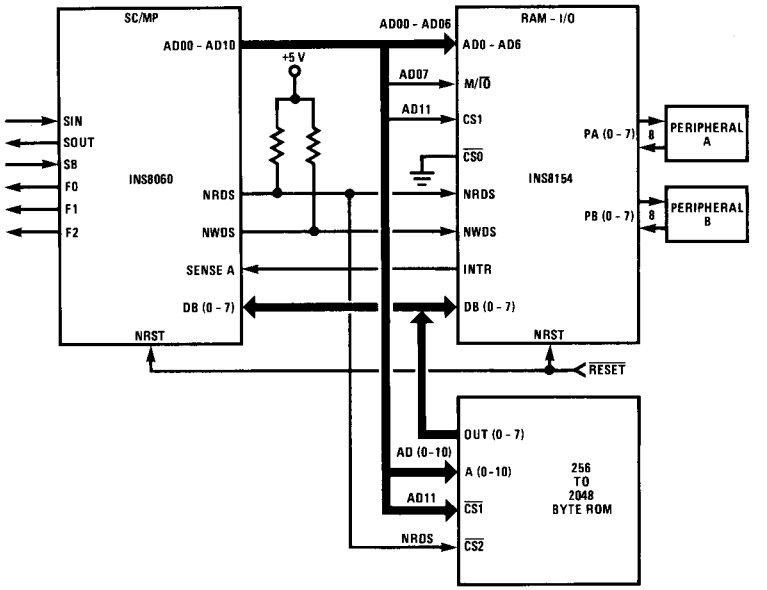


Figure 14. Typical Application – Three-Chip SC/MP System with 128 Bytes of RAM, 22 Bits of I/O and up to 2048 Bytes of ROM

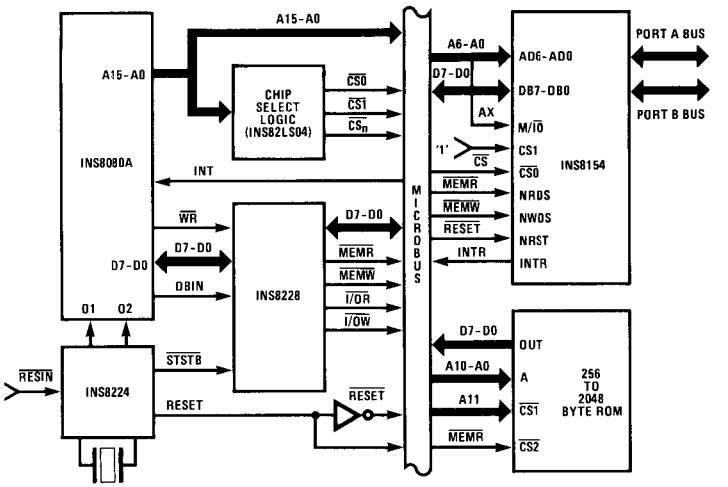
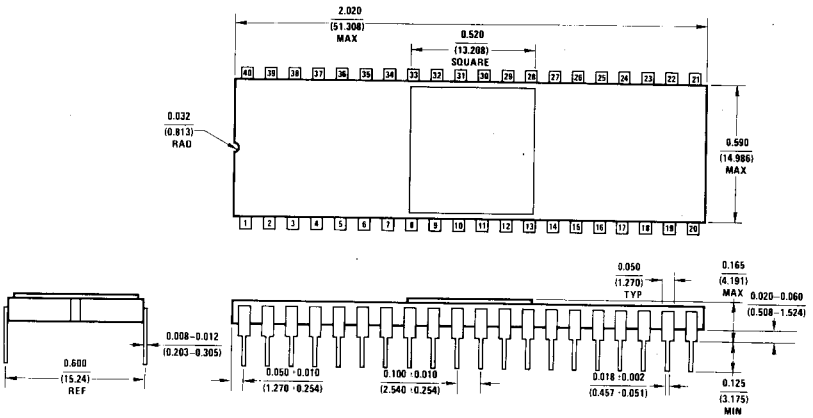
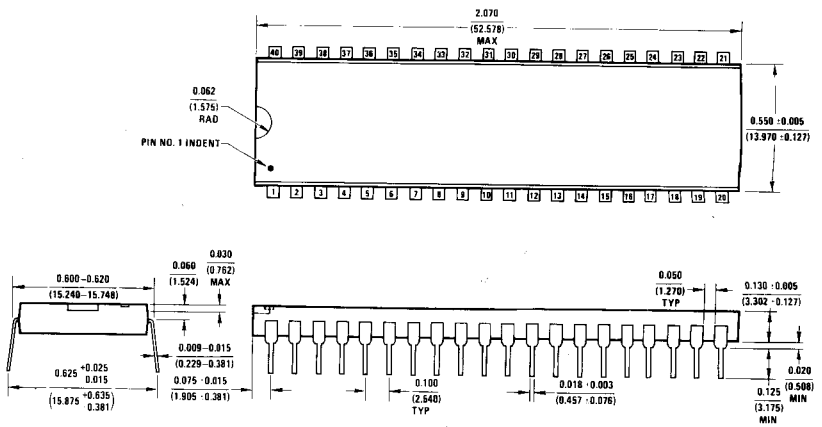


Figure 15. Typical Application – INS8080 System with 128 Bytes of RAM, 16 Bits of I/O and up to 2048 Bytes of ROM

Physical Dimensions



40-Lead Ceramic Dual-in-Line Package (D)
Order Number INS8154D



40-Lead Plastic Dual-in-Line Package (N)
Order Number INS8154N

Ordering Information

The RAM I/O device may be ordered through the local National Semiconductor sales representative or by contacting our world or international headquarters listed below.

For "N" Package: INS8154N
For "D" Package: INS8154D

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, California 95051
Tel. (408) 737-5000
TWX (910) 339-9240

National Semiconductor GmbH
8000 München 21
61/2 Eisenheimerstrasse
West Germany
Tel. 089/9 15027
Telex. 05-22772

NS International Inc., Japan
Miyake Building
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Tokyo, Japan
Tel. (03) 355-3711
TWX 232-2015 NSCJ-J

NS Electronics (Hong Kong) Ltd.
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