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EF9369

ADVANCE INFORMATION

HMOS2

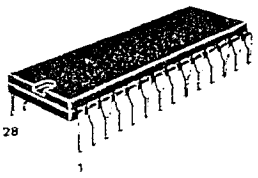
SINGLE CHIP
COLOR PALETTE

SINGLE CHIP COLOR PALETTE

The EF9369 single chip palette provides a low cost, yet dramatic enhancement for any low to mid-range color graphics application. It allows displaying up to 16 different colors, each of these colors being freely selected out of 4096 preset values. EF9369 contains a 16 register color look-up table, three 4-bit D/A converters and a microprocessor interface for color loading.

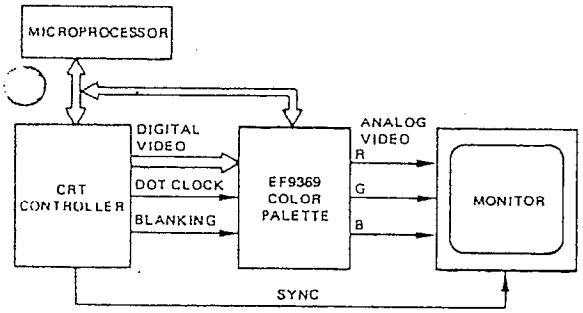
- On chip color look-up table
- 4096 color palette (16 colors selected from 4096)
- On-chip three 4-bit resolution video DACs with γ law correction
- Dot rate up to 17 Megadots per second
- Marking bit for inlay purpose
- Versatile microprocessor interface :
  - directly compatible with address/data multiplexed 8-bit microprocessor bus such as 6801, EF6805CT, 8051...
  - directly compatible with non-multiplexed 8 or 16-bit microprocessor bus (6809, 6502, 68008...).
- Single 5 V supply
- HMOS 2 technology.

CASE CB-132

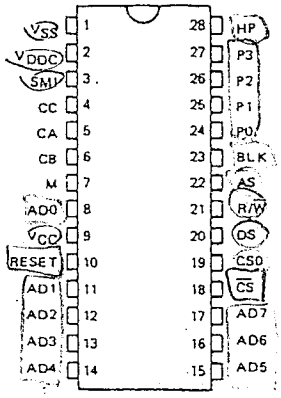


P SUFFIX
PLASTIC PACKAGE

TYPICAL APPLICATION



PIN ASSIGNMENT



Ref 00570 (Replaces SP18402)

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THOMSON COMPONENTS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}*	- 0.3 to 7.0	V
Input voltage	V_{in}*	0.3 to 7.0	V
Operating temperature range	T_A	0 to 70	°C
Storage temperature range	T_{stg}	- 55 to 150	°C
Max power dissipation	P_{Dm}	0.45	W

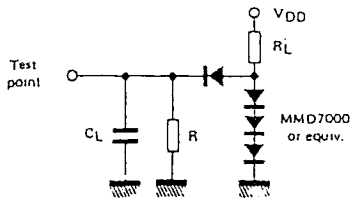
*With respect to V_{SS}

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

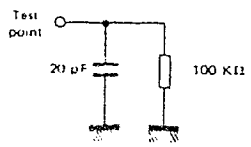
ELECTRICAL CHARACTERISTICS
(V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 to 70°C))

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5	5.25	V
Analog supply voltage	V_{DDC}	–	V_{CC}	TBD	V
Analog supply current	I_{DDC}	–	20	–	mA
Input low voltage	V_{IL}	0.3		0.8	V
Input high voltage	V_{IH}	2		V_{CC}	V
Input leakage current	I_{in}			20	µA
Output high voltage (I_{load} = - 500 µA)	V_{OH}	2.4		–	V
Output low voltage (I_{load} = 1.6 mA)	V_{OL}	–		0.4	V
Power dissipation	P_D		250	–	mW
Input capacitance	C_{in}			15	pF
Three state (off state) input current	I_{TSI}			10	µA

Test load for digital output



Test load for analog output

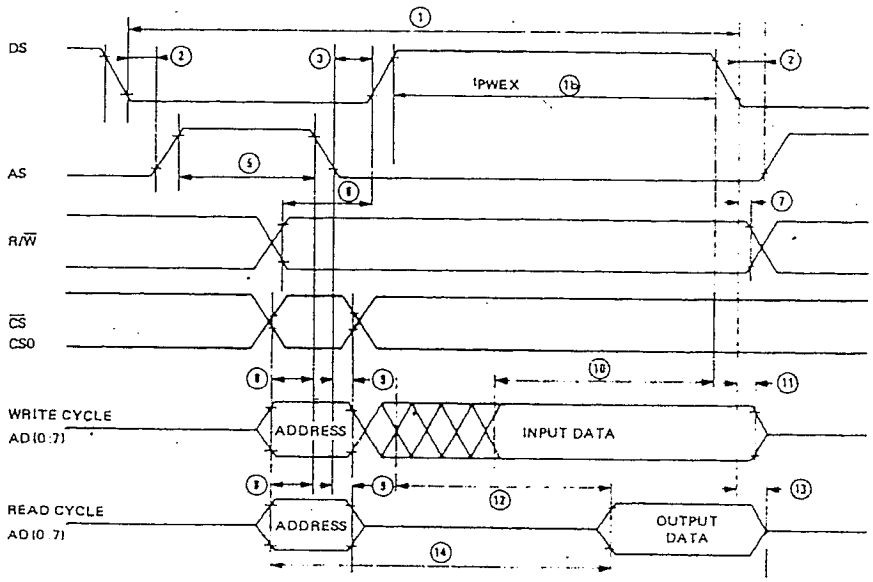


	ADIC71	M
C	100 pF	50 pF
R_L	1 KΩ	3.3 KΩ
R	4.7 KΩ	4.7 KΩ

MICROPROCESSOR INTERFACE TIMING AD(0:7), AS, DS, R/$\overline{W}$, $\overline{CS}$, CS0
V_{CC} = 5.0 ± 5 %, T_A = 0° to + 70°C, C_L = 100 pF on AD(0:7)
Reference levels : V_{IL} = 0.8 V and V_{IH} = 2 V on all inputs ; V_{OL} = 0.4 V and V_{OH} = 2.4 V on all outputs.

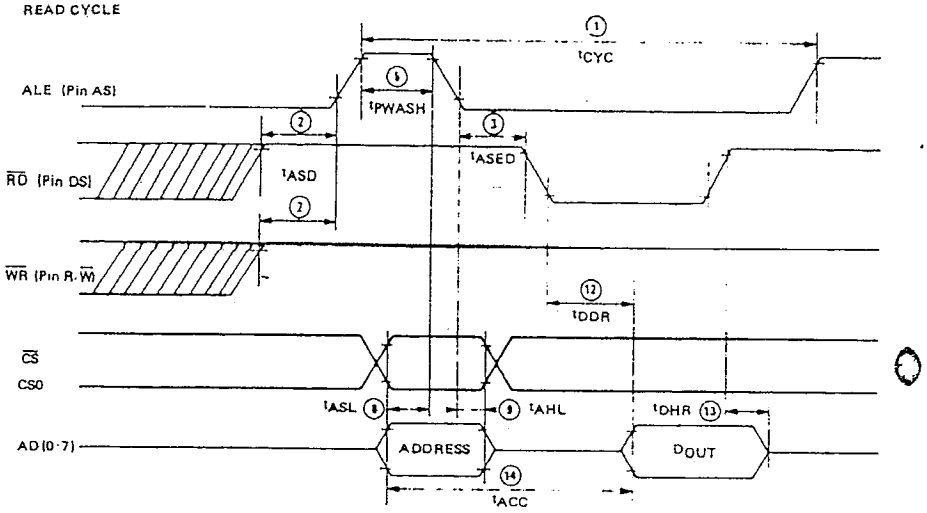
Ident. number	Characteristic	Symbol	Min	Typ	Max	Unit
1	Cycle time	t_{CYC}	400	–	–	ns
1b	DS pulse width high time	t_{PWEX}	200	–	–	ns
1c	DS pulse width low time (Timing 3)	t_{PWEL}	100	–	1000	ns
2	DS low to AS high (timing 1) DS high or R/$\overline{W}$ high to AS high (timing 2)	t_{ASD}	30	–	–	ns
3	AS low to DS high (timing 1) AS low to DS low or R/$\overline{W}$ low (timing 2)	t_{ASED}	30	–	–	ns
4	Write pulse width	t_{PWEH}	200	–	–	ns
5	AS pulse width	t_{PWASH}	100	–	–	ns
6	R/$\overline{W}$ to DS setup time (timing 1)	t_{RWS}	100	–	–	ns
7	R/$\overline{W}$ to DS hold time (timing 1)	t_{RWH}	10	–	–	ns
8	Address and $\overline{CS}$, CS0 setup time	t_{ASL}	20	–	–	ns
9	Address and $\overline{CS}$, CS0 hold time	t_{AHL}	20	–	–	ns
10	Data setup time (write cycle)	t_{DSW}	100	–	–	ns
11	Data hold time (write cycle)	t_{DHW}	10	–	–	ns
12	Data access time from DS (read cycle)	t_{DDR}		–	150	ns
13	DS inactive to high impedance state time (read cycle)	t_{DHR}	10	–	80	ns
14	Address to data valid access time	t_{ACC}		–	300	ns

TIMING DIAGRAM 1 – MULTIPLEXED MODE - MOTOROLA TYPE (SMI - V_{SS})

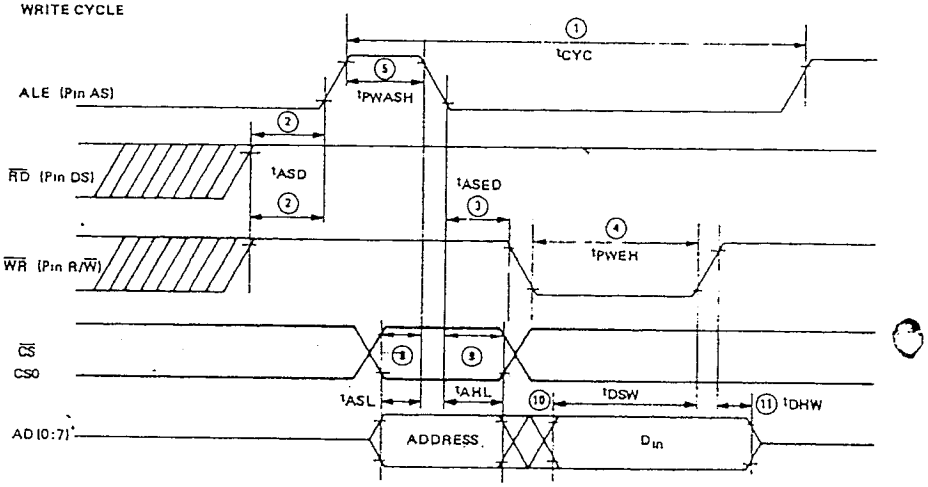


TIMING DIAGRAM 2 – MULTIPLEXED MODE - INTEL TYPE (SMI = V_{SS})

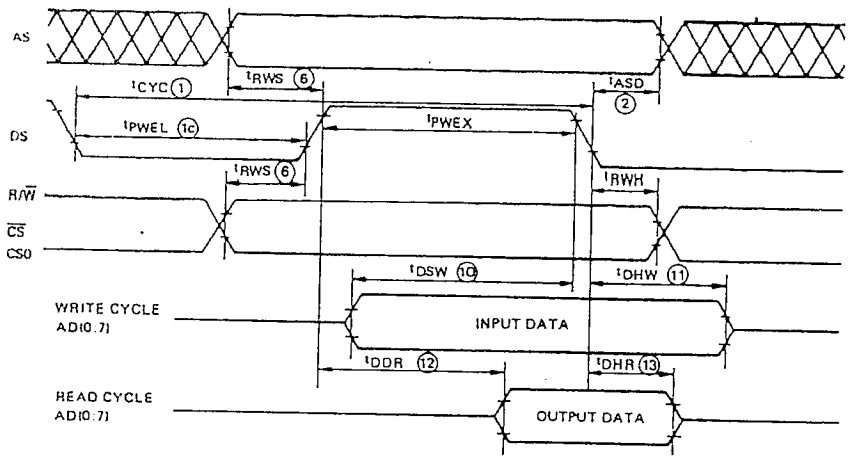
READ CYCLE



WRITE CYCLE



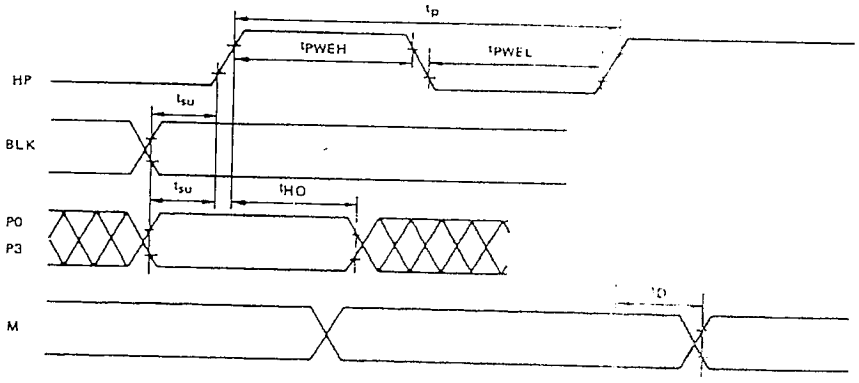
TIMING DIAGRAM 3 – NON-MULTIPLEXED MODE (SMI = V_{CC})



DIGITAL VIDEO SIGNALS - HP, P(0:3), BLK, M. RESET
V_{CC} = 5.0 ± 5 %, T_A = 0°C to + 70°C, C_L = 50 pF on M.
Reference levels : V_{IL} = 0.8 V and V_{IH} = 2 V on all inputs ,
V_{OL} = 0.4 V and V_{OH} = 2.4 V on all outputs

Characteristic	Symbol	Min	Typ	Max	Unit
HP clock period	t_p	50		1000	ns
HP high pulse width	t_{PWEH}	25		-	ns
HP low pulse width	t_{PWEL}	25		-	ns
BLK and P(0:3) set up time to HP	t_{su}	20		-	ns
BLK and P(0:3) hold time from HP	t_{HO}	10		-	ns
M output delay from HP	t_D	-		45	ns
RESET low pulse width	t_{PWRL}	100	-	-	ns

TIMING DIAGRAM 4



ANALOG VIDEO OUTPUTS - CA, CB, CC
V_{DCC} = 5 V, T_A = 0° to+ 70°C, C_L = 20 pF, R_L = 100 kΩ

TABLE 1

Binary input		Analog output (V)		
		Min	Typ	Max
Low level	0000	–	0.8	–
	0001	–	1.18	–
	0010	–	1.28	–
	0011	–	1.36	–
	0100	–	1.42	–
	0101	–	1.47	–
	0110	–	1.52	–
	0111	–	1.56	–
	1000	–	1.60	–
	1001	–	1.63	–
	1010	–	1.66	–
	1011	–	1.69	–
	1100	–	1.72	–
	1101	–	1.75	–
	1110	–	1.76	–
High level	1111	–	1.80	–

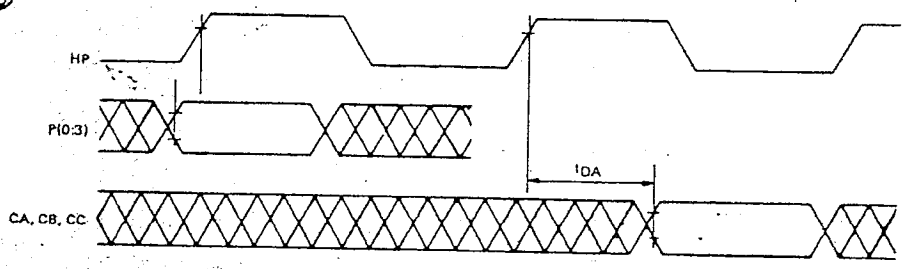
Note :
The internal A/D converters deliver on CA, CB and CC outputs 16 levels with γ law correction (γ = 2.8). The typical transfer characteristic is given by :

$$V = \left(\frac{N}{15}\right)^{\frac{1}{2.8}} \cdot \frac{V_{DDC}}{5} + 0.16\ V_{DCC}$$

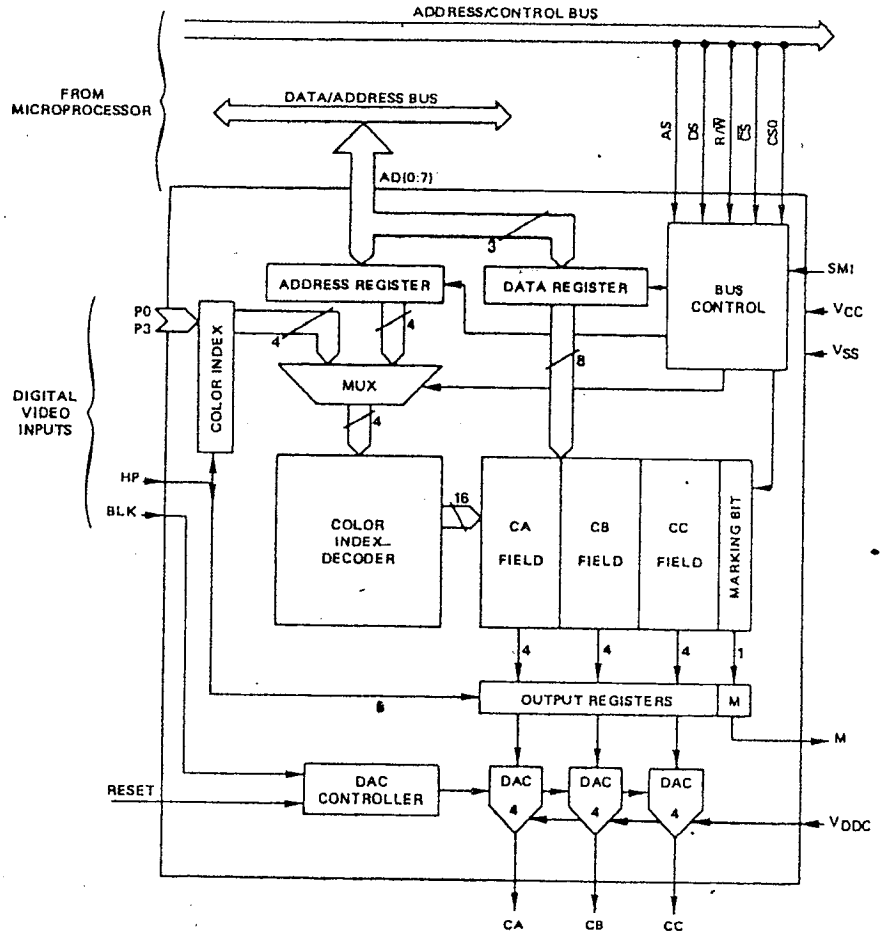
Where N is the binary input value.

Characteristic	Symbol	Min	Typ	Max	Unit
CA, CB, CC outputs from HP	t_{DA}	–	80	–	ns

TIMING DIAGRAM 5



BLOCK DIAGRAM



PIN DESCRIPTION

MICROPROCESSOR INTERFACE
All the input/output pins are TTL compatible.

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
AD(0:7)	I/O	8-11-14 16 - 17	Multiplexed address/data bus	These 8 bidirectional pins are to be connected to the microprocessor system bus.
SMI	I	3	Interface mode select	When this input is connected to V_{CC}, the EF9369 is in the non multiplexed mode. When this input is connected to V_{SS} (ground), the EF9369 is in a multiplexed mode to provide a direct interface with either Motorola or Intel type microprocessor.
AS	I	22	Address strobe	In non-multiplexed mode, this input selects either the address register (AS = 1) or the data register (AS = 0) to be accessed. In multiplexed mode, the falling edge of this control signal latches the address on the AD(0:7) lines, the state of the Data Strobe (DS) and Chip Select lines ($\overline{CS}$, CS0). When using Intel type microprocessor, this input must be connected to the ALE control line.
DS	I	20	Data strobe	In non-multiplexed mode, this active high control signal enables the AD(0:7) input/output buffers and strobes data to/from the EF9369. This signal is usually derived from the processor E (ϕ2) clock. In multiplexed mode, the input is strobed by the falling edge of AS. The strobe value selects either Motorola or Intel type. When using an Intel type microprocessor, DS must be connected to the $\overline{RD}$ control line. With a Motorola type microprocessor, DS must be connected to E(ϕ2) clock.
R/$\overline{W}$	I	21	Read/Write	This control signal determines whether the EF9369 is read (R/$\overline{W}$ = 1) or written (R/$\overline{W}$ = 0). When using Intel type microprocessor, this input must be connected to the $\overline{WR}$ control line.
$\overline{CS}$ CS0	I	18 19	Chip Select	$\overline{CS}$ must be low and CS0 must be high to select the EF9369. In non-multiplexed mode, the EF9369 remains selected as long as the selection condition is met. In multiplexed mode, the selection condition is latched when AS is low.

VIDEO INTERFACE

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
P(0:3)	I	24 - 27	Pixel inputs	These four TTL compatible inputs are strobed by HP into the color index register to address the color look-up table.
HP	I	28	Dot clock	The rising edge of this input latches the P(0:3) and BLK inputs into the EF9369 and the data out of the color look-up table into the output registers.
M	O	7	Marking	This output is synchronised by HP and delivers the marking bit value from the color look-up table.
CA CB CC	O	5 6 4	Color outputs	These three analog high impedance outputs deliver the color signal levels from the internal D/A converters (DAC). The delay between CA, CB, CC outputs and the latched value P(0:3) is one HP clock period plus t_{DA} (see Timing Diagram 5).
BLK	I	23	Blanking	A high level on this input forces the CA, CB, CC and M outputs to low level.
RESET	I	10	Reset	This active high input forces the CA, CB, CC, outputs to low level until the next microprocessor access to the device.

OTHER PINS

V_{CC}	S	9	Power supply	+ 5 V.
V_{DDC}	S	2	Analog power supply	Power supply for the internal DACs. This input can be connected to V_{CC}.
V_{SS}	S	1	Power supply	Ground.

EF9369 contains a 16 register Color Look Up Table (CLUT). Each of these 13-bit register holds three 4-bit color fields CA (0:3), CB (0:3) and CC (0:3) and a marking bit M.

These registers can be accessed (read or written) by the microprocessor through the microprocessor interface. These registers are also read by the video process : a 4 bit pixel value and a clock must be provided at pixel rate to the P(0:3) and HP input pins. These signals may be delivered either by 4 video shift registers and the shifting clock of a bit map CRT controller or by an alphanumeric or semi-graphic CRT controller. The pixel value, after clock re-synchronisation, is used as a color index : it selects one out of the 16 CLUT registers. Each color field of the selected register is converted to an analog signal and delivered to one of the CA, CB or CC output. The marking bit is directly routed to the M output. When the CA, CB and CC outputs are used as RGB analog signals, one color out of 4096 is associated to each pixel value. In short this process freely maps a 16 color index set into a 4096 color set.

MICROPROCESSOR INTERFACE

The 8-bit microprocessor interface gives access (read or write) to the CLUT which is addressed as a 32 byte table. The 13-bit color register # N (N = 0 to 15) is accessed at address 2N and 2N + 1. Even address holds CA (0:3) and CB (0:3), next address holds CC (0:3) and M (see fig 1).

EF9369 provides two bus modes through the SMI programming pin :

- Multiplexed mode for address/data multiplexed 8-bit microprocessor bus.
- Non multiplexed mode for non-multiplexed 8 or 16-bit microprocessor bus.

MULTIPLEXED MODE (SMI connected to V_{SS})

In this mode, EF9369 can be directly connected to popular address/data multiplexed microprocessor, either Motorola type (6801, EF6805CT...) or Intel type (8048, 8051, 8088...). In this last case the EF9369 AS, DS and R/$\overline{W}$ inputs must be connected respectively to the ALE, $\overline{RD}$ and $\overline{WR}$ microprocessor control lines.

FIGURE 1 – CLUT ADDRESSING

Color Look-Up Table (CLUT)								CLUT Byte Address								Register Index
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	#
CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	X	X	X	0	0	0	0	0	0
X	X	X	M	CC3	CC2	CC1	CC0	X	X	X	0	0	0	0	1	
CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	X	X	X	0	0	0	1	0	1
X	X	X	M	CC3	CC2	CC1	CC0	X	X	X	0	0	0	1	1	
CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	X	X	X	1	1	1	1	0	15
X	X	X	M	CC3	CC2	CC1	CC0	X	X	X	1	1	1	1	1	

X = don't care.

NOTE : Reading the address register can destroy the CLUT contents.

In this mode, EF9369 maps into the microprocessor addressing space as 32 CLUT byte address. Random access to one byte takes one cycle : on the falling edge of the AS input, EF9369 latches AD (0:7) into the on-chip address register, the DS and chip select lines into dedicated flip-flops. The strobed value of DS allows recognition of Intel or Motorola type for further processing. (See pin description section and microprocessor timing diagrams for details). When the EF9369 chip select lines enable selection, the addressed byte is accessed during the data phase of the cycle.

NON MULTIPLEXED MODE (SMI connected to V_{CC})

In this mode EF9369 can be directly connected to any 8 or 16-bit, non multiplexed, microprocessor bus (6800, 6809, 6502, 68008...).

This mode provides an Indirect, auto-incremented addressing scheme. EF9369 maps into the microprocessor addressing space as 2 byte address only. AS is used to select one out of 2 registers :

- the write only address register (5 bits) addressed when AS = 1.
- the read/write data register (8 bits) addressed when AS = 0.

Random access to a CLUT byte takes two bus cycles : 1/ Load the CLUT address into the address register. 2/ Access (read or write) the value in the data register.

After each access to the data register, the address register is automatically incremented modulo 32. This scheme allows sequential addressing to the CLUT without address reloading, the complete CLUT can so be reloaded in 33 bus cycles.

VIDEO PROCESS

The CRT controller sends to EF9369 a pixel value on pins P (0:3), a pixel rate clock on HP input and a blanking signal on pin BLK. The pixel value is latched into the color index register by the rising edge of HP. The color index register selects one register in the CLUT. The color fields of the selected register are routed to 3 DACs and M is directly routed to the M digital output.

After impedance matching, the CA, CB and CC outputs can be used to drive a RGB analog color monitor. Alternatively one of these outputs can be used to drive a monochrome monitor thus providing up to 16 gray levels. The marking digital output can be used to drive external video switches, thus providing video overlay facility on a color per color basis.

The blanking input forces the analog outputs and the M output to low level thus allowing the beam to be switched off during retrace intervals.

NOTES

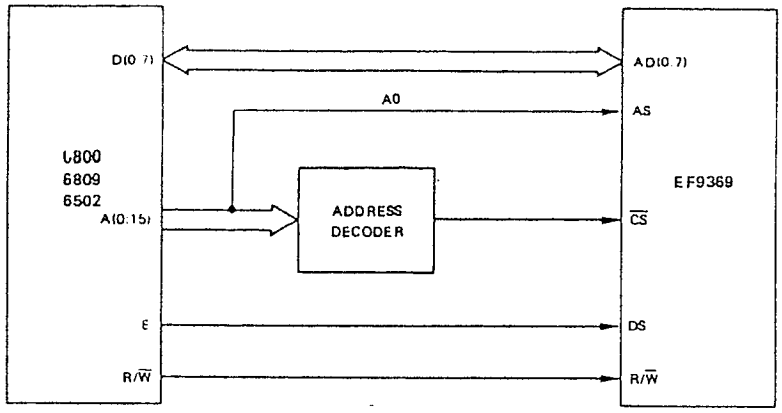
1. Each 4 bit-D/A converter is γ corrected in order to linearize the luminance driven on the screen versus the digital value. The typical digital to voltage conversion law is given table 1. The output voltages are proportionnal to the analog supply voltage V_{DDC}. When required, setting V_{DDC} allows a gain adjustment. But in most applications, V_{DDC} and V_{DD} can be derived from the same supply through independent decoupling.

2. CA, CB and CC are high impedance outputs (500 Ω typical) which require proper adaptation in most applications. THOMSON SEMICONDUCTORS TEA 5114 provides such a 1 V - 75 Ω low cost adaptation (See fig. 2).

3. As the CLUT is shared between microprocessor access and video access, a low level is forced on the CA, CB, CC and M outputs during any chip select periods. To avoid to spoil the screen with black strokes it is recommended to access the CLUT from the microprocessor only during the retrace periods.

4. RESET - This input forces CA, CB, CC and M outputs to a low level until the next microprocessor access. At power on or at the beginning of a session RESET allows to keep a clean black screen until proper initialization.

INTERFACE WITH 6800/6809 TYPE MICROPROCESSOR



INTERFACE WITH EF6805CT

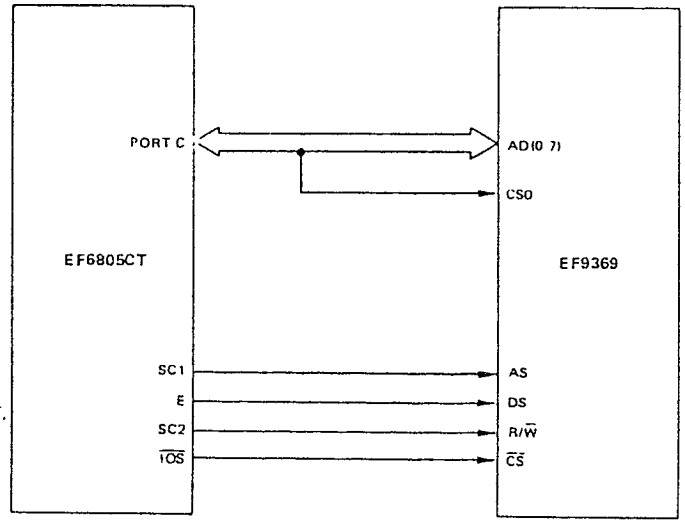
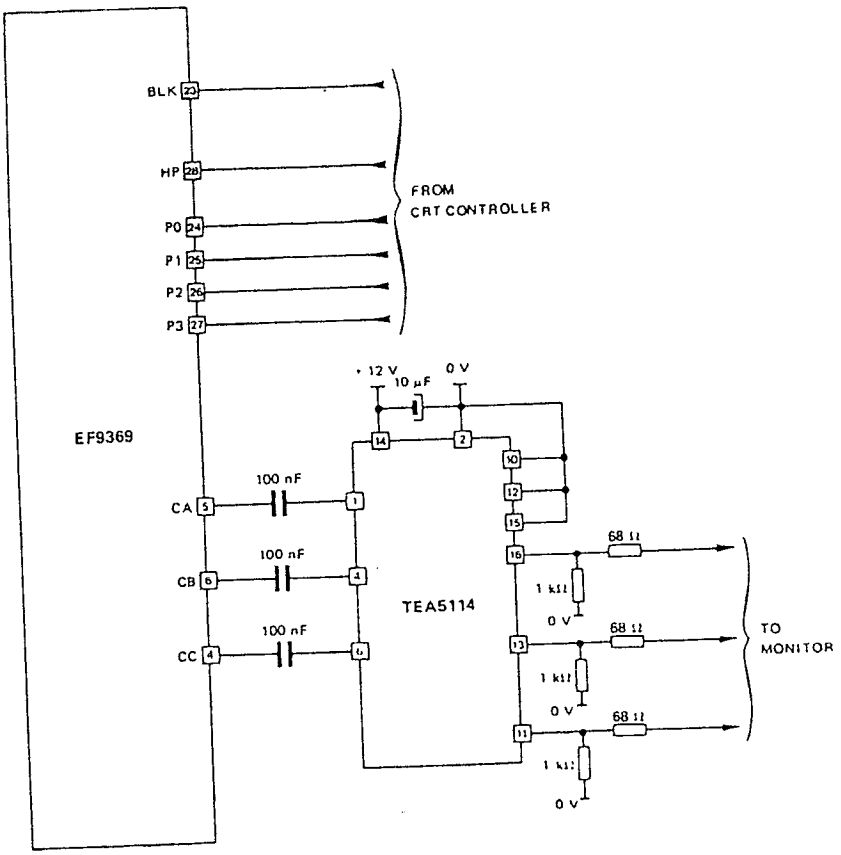
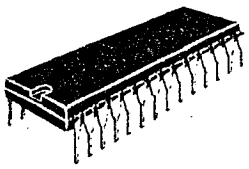


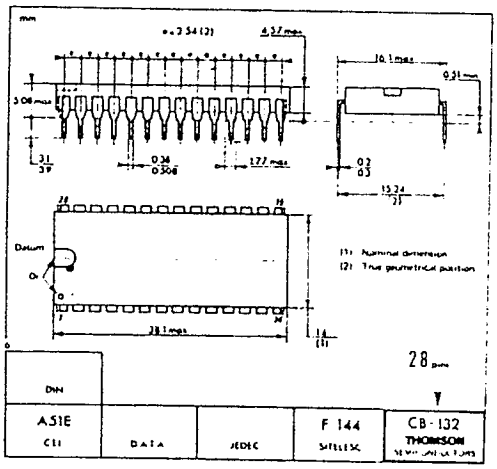
FIGURE 2 - TYPICAL TV (S-) VIDEO INTERFACE



CASE CB-132



P SUFFIX
PLASTIC PACKAGE



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