ITT4116
16384-Bit Dynamic Random Access Memory

Refresh 128 every 2MS

290
2860

002860

ORIG

ITT

6251-121-5E

semiconductors ITT

16384-Bit Dynamic Random Access Memory

Features

- Industry standard 16 pin DIP
- 150 ns access time (ITT 4116–2)
- 200 ns access time (ITT 4116–3)
- 250 ns access time (ITT 4116–4)
- All inputs including clocks are TTL compatible
- Standard power supplies, +12V, +5V, −5V with ± 10% tolerance
- Three state TTL compatible output, Data out is not latched
- Page mode capability
- Addresses and data in have on-chip latches
- Pin and function compatible with Mostek MK 4116

General

The ITT 4116 is a 16384 word by one bit random access memory fabricated with ITT's N-channel double-poly coplanar silicon gate process for high performance and high functional density. A single transistor dynamic storage cell and dynamic balanced sense amplifiers as used in the ITT 4116 achieve high speed with low power dissipation.

Packaging of the ITT 4116 in the industry standard 16 pin package is made possible by multiplexing the 14 address bits (required to address 1 of 16384 bits) into the ITT 4116 on 7 address input pins (A_0-A_6). Two TTL clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), latch the two 7 bit address words into the ITT 4116. The 16 pin DIP gives the highest system bit densities and can be handled with widely available automatic testing and insertion equipment.

Several operating modes are incorporated in the ITT 4116 in addition to the usual read and write cycles; read modify write, page mode and $\overline{RAS}$ only refresh cycles are available.

The ITT 4116 16384 bit memory has the same pin layout as the industry standard ITT 4027 4096 bit memory with the exception of chip select which is replaced by an additional address input needed to accommodate 16384 bits.

Absolute Maximum Ratings*

Voltage on any pin relative to V_{BB}	−0.5V to +20V
Voltage on V_{DD}, V_{CC} relative to V_{SS}	−1.0V to +15V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS}>0$)	0V
Operating temperature, T_A (Ambient)	0°C to +70°C
Storage temperature (Ambient)	−65°C to +150°C
Short Circuit Output Current	50mA
Power dissipation	1 Watt

* Exposure to absolute maximum conditions for extended periods may affect device reliability.

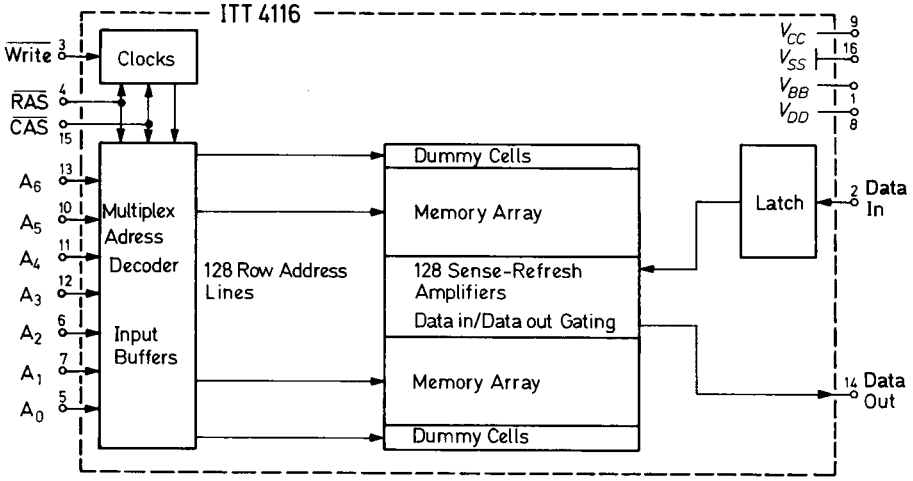

Fig. 1: Block Diagram

Package Description

The ITT 4116 is available in two different package versions:

- in a cerdip 16 pin glass sealed ceramic package, weight approx. 2 g, suffix D to the type number
- in a 16 pin plastic package, weight approx. 1.2 g, suffix N to the type number

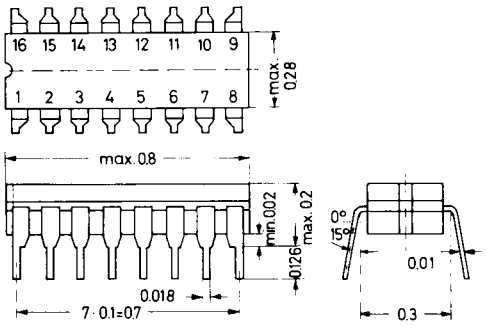

Fig. 2a: Cerdip Package (Suffix D)

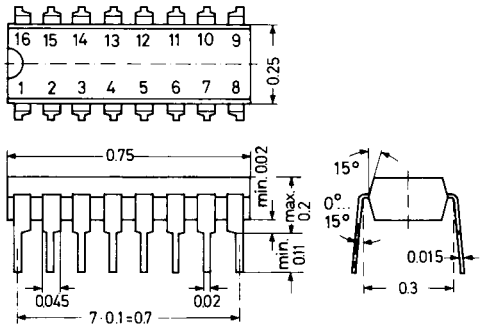

Fig. 2b: Plastic Package (Suffix N)

All Dimensions in inches

Pin Connections

1	Supply Voltage V_{BB}	9	Supply voltage V_{CC}
2	Input Data in	10	Address input A_5
3	$\overline{\text{WRITE}}$ input	11	Address input A_4
4	$\overline{\text{RAS}}$ input	12	Address input A_3
5	Address input A_0	13	Address input A_6
6	Address input A_2	14	Output Data out
7	Address input A_1	15	$\overline{\text{CAS}}$ input
8	Supply voltage V_{DD}	16	Supply voltage V_{SS}

Recommended DC Operating Conditions[4] ($0\ °C \leq T_A \leq 70\ °C$)[1]

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{DD}	10.8	12.0	13.2	volts	2
Supply Voltage	V_{CC}	4.5 V	5.0	5.5	volts	2,3
Supply Voltage	V_{SS}	0	0	0	volts	2
Supply Voltage	V_{BB}	–4.5	–5.0	–5.7	volts	2
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7	–	7.0	volts	2
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.4	–	7.0	volts	2
Logic 0 Voltage, all inputs	V_{IL}	–1.0	–	0.8	volts	2

DC Electrical Characteristics[4] ($0\ °C \leq T_A \leq 70\ °C$)[1] ($V_{DD} = 12\ V \pm 10\%$; $V_{CC} = 5\ V \pm 10\%$; $V_{SS} = 0\ V$; $V_{BB} = -4.5\ V$ to $-5.7\ V$)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Operating Current						
Average power supply operating current	I_{DD1}	–	–	35	mA	5
$\overline{RAS}$, $\overline{CAS}$ cycling: $t_{RC} = t_{RC}$ (min)	I_{CC1}	–	–	–	–	6
	I_{BB1}	–	–	200	μA	–
Standby current						
Power supply standby current	I_{DD2}	–	–	1.5	mA	18
($\overline{RAS} = V_{IHC}$)	I_{CC2}	–10	–	10	μA	–
	I_{BB2}	–	–	100	μA	–
Refresh Current						
Average power supply current,	I_{DD3}	–	–	27	mA	5, 18
refresh mode	I_{CC3}	–10	–	10	μA	–
($\overline{RAS}$ cycling, $t_{RC} = t_{RC}$ (min)	I_{BB3}	–	–	200	μA	–
Page Mode Current						
Average power supply current,	I_{DD4}	–	–	27	mA	5
page mode operation	I_{CC4}	–	–	–	–	6
($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ (min)	I_{BB4}	–	–	200	μA	–
Input Leakage Current any input ($V_{BB} = -5\ V$, $0\ V \leq V_{IN} \leq +7.0\ V$, all other pins not under test = 0 volts)	I_{IL}	–10	–	10	μA	–
Output Leakage Current	I_{OL}	–10	–	10	μA	18, 19
Output Levels						
Output high (Logic 1) voltage ($I_{OUT} = -5$ mA)	V_{OH}	2.4	–	–	volts	3
Output low (Logic 0) voltage ($I_{OUT} = 4.2$ mA)	V_{OL}	–	–	0.4	volts	–

AC Electrical Characteristics ($0\,°C \leq T_A \leq 70\,°C$) ($V_{DD} = 12.0\,V \pm 10\%$; $V_{SS} = 0\,V$; $V_{BB} = -4.5\,V$ to $-5.7\,V$)

Parameter	Symbol	Typ.	Max.	Units	Notes
Input Capacitance (A_0–A_6), D_{IN}	C_{11}	4	5	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{12}	8	10	pF	17
Output Capacitance (D_{OUT})	C_O	5	7	pF	17,18

Electrical Characteristics and Recommended AC Operating Conditions (Notes 4, 7, 11)

($0\,°C \leq T_A \leq 70\,°C$)[1] ($V_{DD} = 12.0\,V \pm 10\%$; $V_{CC} = 5.0\,V \pm 10\%$; $V_{SS} = 0\,V$, $V_{BB} = -4.5\,V$ to $-5.7\,V$)

Parameter	Symbol	ITT 4116-2		ITT 4116-3		ITT 4116-4			
		Min.	Max.	Min.	Max.	Min.	Max.	Units	Notes
Random read or write cycle time	t_{RC}	320	–	375	–	410	–	ns	8
Read write cycle time	t_{RWC}	320	–	375	–	425	–	ns	8
Read modify write cycle time	t_{RMW}	320	–	405	–	500	–	–	–
Page mode cycle time	t_{PC}	170	–	225	–	275	–	ns	–
Access time from $\overline{RAS}$	t_{RAC}	–	150	–	200	–	250	ns	9,12
Access time from $\overline{CAS}$	t_{CAC}	–	100	–	135	–	165	ns	10,12
Output buffer turn-off delay	t_{OFF}	0	40	0	50	0	60	ns	13
Transition time (rise and fall)	t_T	3	35	3	50	3	50	ns	7
$\overline{RAS}$ precharge time	t_{RP}	100	–	120	–	150	–	ns	–
$\overline{RAS}$ pulse width	t_{RAS}	150	10,000	200	10,000	250	10,000	ns	–
$\overline{RAS}$ hold time	t_{RSH}	100	–	135	–	165	–	ns	–
$\overline{CAS}$ hold time	t_{CSH}	150	–	200	–	250	–	ns	–
$\overline{CAS}$ pulse width	t_{CAS}	100	–	135	–	165	–	ns	–
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	65	35	85	ns	14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	–20	–	–20	–	–20	–	ns	–
Row Address set-up time	t_{ASR}	0	–	0	–	0	–	ns	–
Row Address hold time	t_{RAH}	20	–	25	–	35	–	ns	–
Column Address set-up time	t_{ASC}	–10	–	–10	–	–10	–	ns	–
Column Address hold time	t_{CAH}	45	–	55	–	75	–	ns	–
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	95	–	120	–	160	–	ns	–
Read command set-up time	t_{RCS}	0	–	0	–	0	–	ns	–
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	–
Write command hold time	t_{WCH}	45	–	55	–	75	–	ns	–
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	95	–	120	–	160	–	ns	–
Write command pulse width	t_{WP}	45	–	55	–	75	–	ns	–
Write command to $\overline{RAS}$ lead time	t_{RWL}	50	–	70	–	85	–	ns	–
Write command to $\overline{CAS}$ lead time	t_{CWL}	50	–	70	–	85	–	ns	–
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	15
Data-in hold time	t_{DH}	45	–	55	–	75	–	ns	15
Date-in hold time referenced to $\overline{RAS}$	t_{DHR}	95	–	120	–	160	–	ns	–
$\overline{CAS}$ precharge time (for page-mode cycle only)	t_{CP}	60	–	80	–	100	–	ns	–
Refresh period	t_{REF}	–	2	–	2	–	2	ms	–
$\overline{WRITE}$ command set-up time	t_{WCS}	–20	–	–20	–	–20	–	ns	16
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	60	–	80	–	90	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	110	–	145	–	175	–	ns	16

Notes

1. T_A is specified for operation at frequencies $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met.

2. All voltages referenced to V_{SS}.

3. Output Voltage will swing from V_{SS} to V_{CC} when enabled, with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

4. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

5. Current is proportional to cycle rate. I_{DD1} (max), I_{DD3} (max) and I_{DD4} are measured at the cycle rate specified by t_{RC} (min).

6. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to Data out. At all other times I_{CC} consists of leakage currents only.

7. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

8. The specifications for t_{RC} (min) and t_{RWC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0 °C $\leq T_A \leq$ 70 °C) is assured.

9. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

10. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

11. AC measurements assume $t_T = 5$ ns.

12. Measured with a load equivalent to 2 TTL loads and 100 pF.

13. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

15. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify write cycles.

16. t_{WCS}, t_{WCD} and t_{RWD} are restrictive operating parameters in R·W and RMW cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the Data Out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the Data Out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the Data Out (at access time) is indeterminate.

17. Effective capacitance calculated from the equation
$$C = \frac{I \cdot \triangle t}{\triangle V}$$
with $\triangle V = 3$ volts and power supplies at nominal levels.

18. $\overline{CAS} = V_{IHC}$ to disable D_{OUT}.

19. $0 V \leq V_{OUT} \leq +5.5 V$.

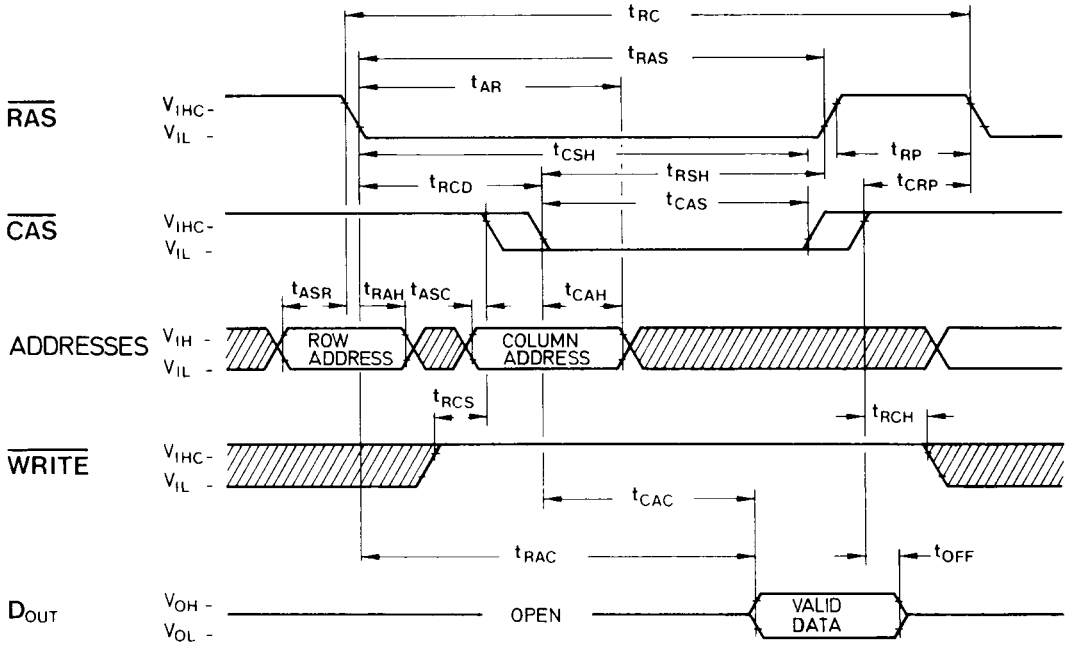

Fig. 3: Read Cycle

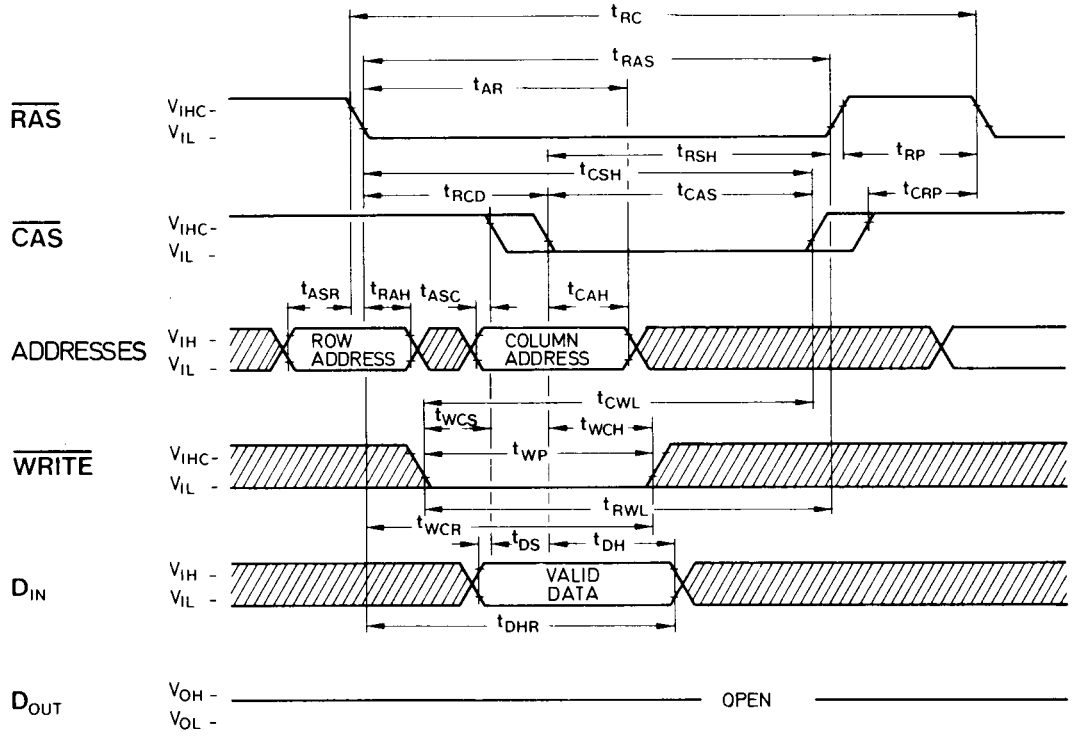

Fig. 4: Write Cycle (Early Write)

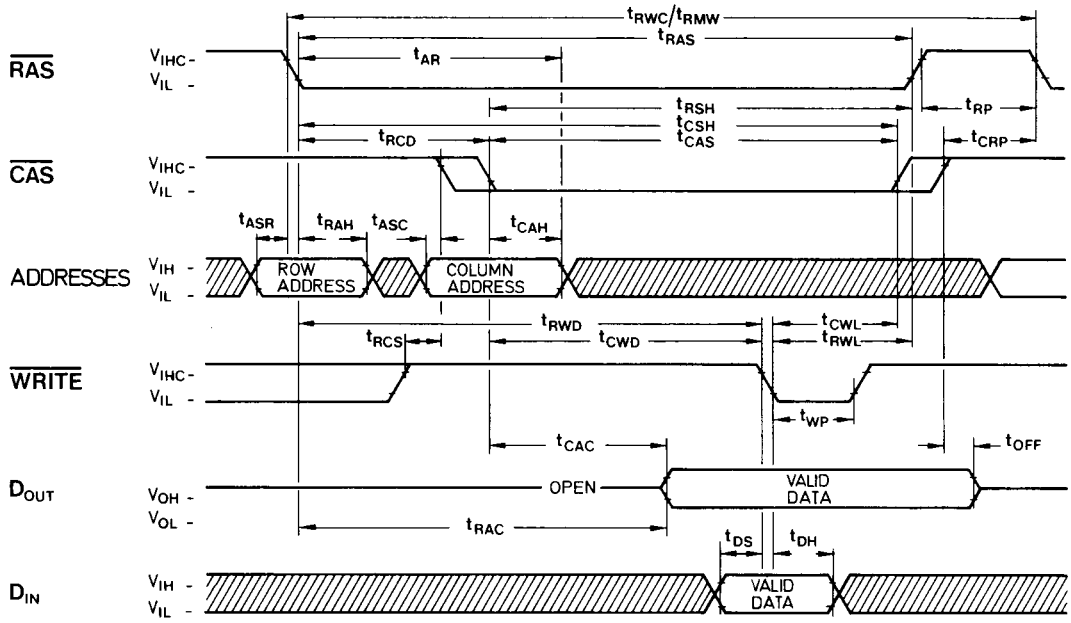

Fig. 5: Read–Write/Read–Modify–Write Cycle

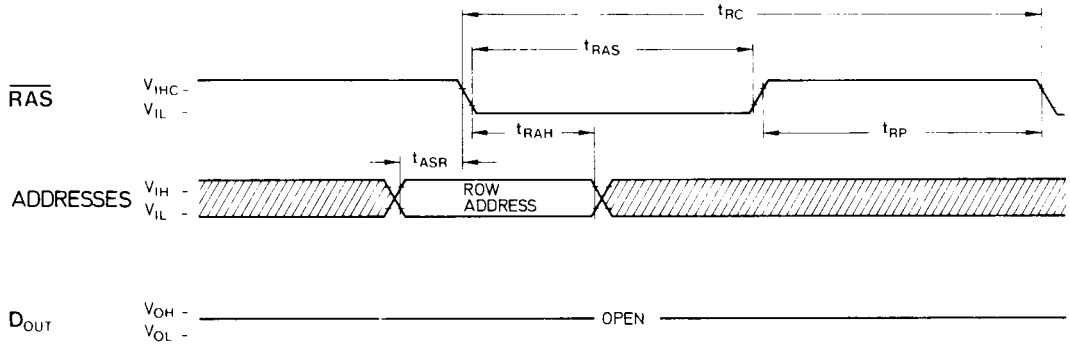

Fig. 6: "$\overline{\text{RAS}}$–Only" Refresh Cycle
Note: $\overline{\text{CAS}}$ = V_{IHC}, $\overline{\text{WRITE}}$ = Don't Care

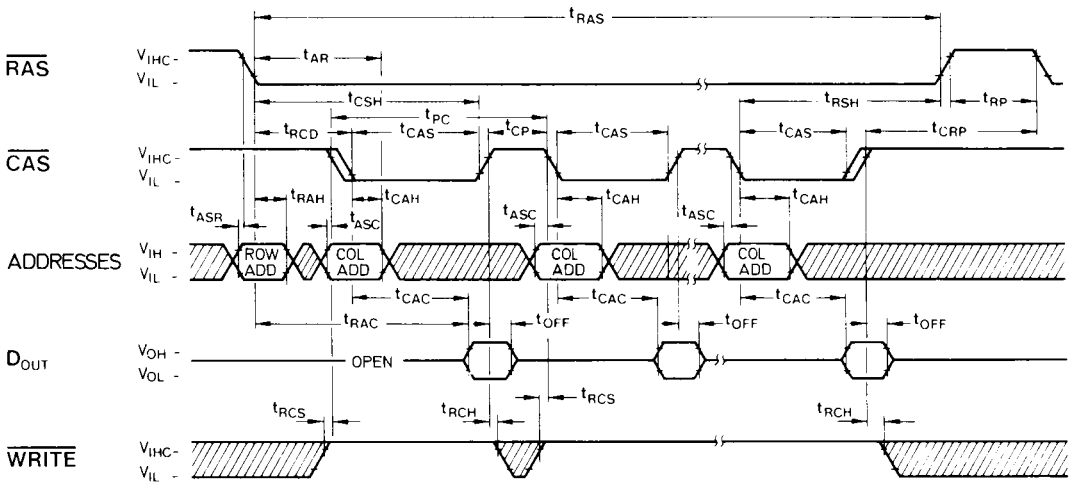

Fig. 7: Page Mode Read Cycle

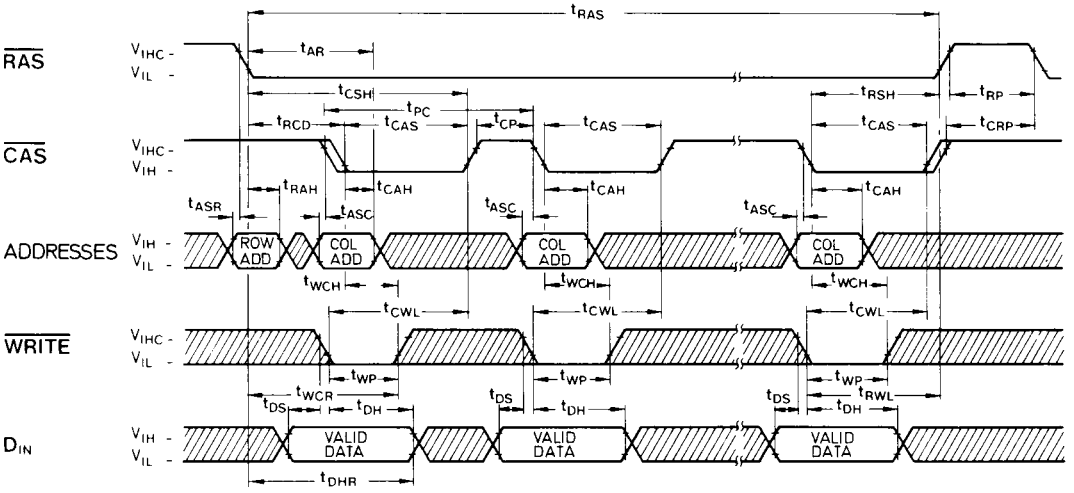

Fig. 8: Page Mode Write Cycle

Addressing

Fourteen address bits are necessary to decode 1 of the 16384 cell locations and these are multiplexed on to the seven address inputs of the ITT 4116. Two externally applied negative going TTL clock pulses latch these inputs into on-chip address latches. Row Address Strobe ($\overline{RAS}$), the first clock, latches the 7 row address bits, and then Column Address Strobe ($\overline{CAS}$), the 7 column address bits. An internal clock chain is triggered by $\overline{RAS}$ and another by $\overline{CAS}$; these two logically linked clock chains control the address multiplexing operation so that it occurs outside the critical path timing sequence for read data access. The "gated $\overline{CAS}$" feature, that is the internal inhibition of the $\overline{CAS}$ clock chain until the occurrence of a delayed signal from the $\overline{RAS}$ clock chain, allows the $\overline{CAS}$ clock pulse to be applied immediately the Row address information has been changed to Column address information provided the Row Address Hold Time (t_{RAH}) specification has been met. Any delay in applying $\overline{CAS}$ after t_{RAH} will not affect the worst case data access time (t_{RAC}) provided $\overline{CAS}$ occurs before the delayed signal from the $\overline{RAS}$ clock chain. This window for $\overline{CAS}$ with no delay in t_{RAC} is delineated by two timing endpoints t_{RCD} (min) and t_{RCD} (max). If $\overline{CAS}$ is applied after t_{RCD} (max), no data storage or reading errors will result; however, the access time will be determined from $\overline{CAS}$ access time t_{CAC} and therefore t_{RAC} will be increased by the amount that the actual t_{RCD} exceeds the endpoint t_{RCD} (max).

Data Input/Output

Input data for an addressed cell is latched into an on-chip register when the three negative clocks $\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$ are active. The strobe for the Data In (D_{IN}) register is the negative edge of either $\overline{CAS}$ or $\overline{WRITE}$, whichever is the later, thus permitting various write cycle timing options. If the $\overline{WRITE}$ edge occurs first, D_{IN} is strobed by $\overline{CAS}$ and set-up and hold times are referenced to $\overline{CAS}$. In the case of a read-write cycle or if the data is not available at $\overline{CAS}$, then the D_{IN} is strobed by the delayed $\overline{WRITE}$ edge and set-up and hold times are referenced to $\overline{WRITE}$. "Delayed write" is depicted in the read-write and page mode write cycle timing diagrams and "early write" in the write cycle diagram.

Output of data from an addressed cell is achieved within the specified access time whilst $\overline{WRITE}$ is held inactive or high during the period $\overline{CAS}$ is active.

Data Output Control

Data Output (D_{OUT}) of the ITT 4116 is tri-state TTL compatible and is normally high impedance (i.e. open-circuit and floating). During a read cycle, the output will turn on to either logic 1 or logic 0 at the access time when $\overline{CAS}$ is activated (low level). The valid output data will remain until $\overline{CAS}$ is taken high.

In the case of a read, read-modify-write, or delayed write cycle, D_{OUT} contains the data read from the addressed cell after the access time; this data is the same polarity (not inverted) as the input data. Having gone active the validity of data until $\overline{CAS}$ goes high is unaffected by the subsequent state of $\overline{RAS}$.

If the cycle is "early write" ($\overline{WRITE}$ active before $\overline{CAS}$) then D_{OUT} remains in the high impedance state throughout the cycle. The effect of this mode of operation is that the user can control the data output by the position of the $\overline{WRITE}$ edge during a write cycle and the pulse width of $\overline{CAS}$ during read.

Output control of this nature results in important system operations:

Common I/O operation:
D_{IN} can be connected directly to D_{OUT} giving a common I/O data bus, provided all write operations are in the "early write" mode.

Data Output Control:
D_{OUT} contains valid data during a read cycle from t_{CAC} until $\overline{CAS}$ goes inactive, this allows data to remain valid until the beginning of a subsequent cycle without increasing overall memory cycle time. Thus flexible $\overline{RAS}$ / $\overline{CAS}$ timing relationships are possible.

Chip Selection:
As D_{OUT} is not latched, $\overline{CAS}$ is not required to turn off the outputs of unselected devices. Two methods of chip select are possible by decoding $\overline{CAS}$ and/or $\overline{RAS}$. If both are decoded then a two dimensional chip select array is possible.

Extended Page Boundary:
In page mode operation, multiple column locations are accessed using the same row address in successive memory cycles. If $\overline{CAS}$ is decoded as a page cycle select signal, the page boundary can be extended beyond the 128 column locations of an individual chip.

Output Interfacing

The data output buffer has a low impedance to V_{CC}, 420 Ω maximum (135 Ω typically), for logic state "1" and a low impedance to V_{SS}, 95 Ω maximum (35 Ω typically), for logic state "0". Power to the output buffer can be supplied at the supply voltage of interfacing chips using the separate V_{CC} pin. In standby battery operation, refresh operation of the ITT 4116 is unaffected by removal of power to this separate V_{CC}, thus all system logic except $\overline{RAS}$ timing circuitry and the refresh address logic may be turned off, minimising power requirements.

Page Mode Operation

Multiple column locations may be accessed using the same row address in successive memory cycles; this page mode of operation of the ITT 4116 gives increased speed without increased power. Power is reduced as the $\overline{RAS}$ is kept active (logic "0") after the initial strobe on the first cycle so eliminating the power required on the negative edge of $\overline{RAS}$. Additionally, access and cycle times are reduced by the elimination of time required for strobing the new row.

A single ITT 4116 limits the page boundary to the 128 columns available; however, when more than 16K words are used in a system, the use of $\overline{CAS}$ as a chip select signal extends the page boundary. $\overline{RAS}$ is applied to all devices and $\overline{CAS}$ is decoded as a page cycle select signal: only those devices receiving both $\overline{RAS}$ and $\overline{CAS}$ will perform memory cycles.

Refresh

The dynamic cell matrix requires refresh within every 2 milliseconds at each of the 128 row addresses. Although any memory cycle will achieve this refresh, substantial power savings can easily be made by using $\overline{RAS}$-only cycles as can be seen from the I_{DD3} specification.

Power Considerations

The ITT 4116 consists mainly of dynamic circuitry and most power is consumed on address strobe edges. Power, therefore, is a function of operating frequency rather than active duty cycle (see Fig. 5). Additionally destruction of the device will not result from the clock inputs accidentally becoming grounded.

Provided supply voltages are within specification, no special power noise restrictions are necessary, although adequate decoupling should be provided to suppress high frequency transients to ensure optimum reliability and system performance. As the ITT 4116 draws very little DC power there is minimal need for large capacitors.

For systems requiring low power dissipation, it is necessary to reduce the operation frequency. For example, if the cycle time is 1 microsecond, the operating current will be 20 mA maximum rather than the 35 mA for 375 ns cycle time. Conversely it may be possible for some ITT 4116 to operate with shorter cycle times than 375 ns, provided all AC requirements are met; however, the increased power dissipation will require a reduction in ambient temperature.

Minimum overall system power requirements are achieved if $\overline{RAS}$ as opposed to $\overline{CAS}$ is used to chip select as unselected devices then are in low power (standby) mode regardless of $\overline{CAS}$.

Power Up

The ITT 4116 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to ensure compliance with the Absolute Maximum Ratings, ITT recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and Data Out to the inactive state.

After power is applied to the device, the ITT 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

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