DRAM

1 MEG x 1 DRAM

STANDARD OR LOW POWER, EXTENDED REFRESH

FEATURES

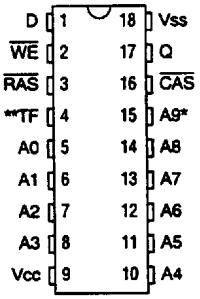
- 512-cycle refresh in 8ms (MT4C1024) or 64ms (MT4C1024 L)
- Industry-standard x1 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 0.8mW standby; 175mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and Extended (MT4C1024 L)
- Low CMOS Standby Current, 200µA maximum (MT4C1024 L)

OPTIONS / MARKING

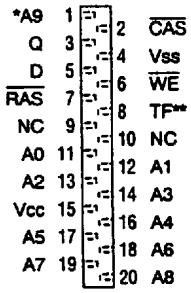
- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Plastic DIP (300 mil) — None
  - Plastic SOJ (300 mil) — DJ
  - Plastic ZIP (350 mil) — Z
- Version
  - 1,024-cycle refresh in 8ms — None
  - 1,024-cycle refresh in 64ms — L
- Part Number Example: MT4C1024DJ-7 L

PIN ASSIGNMENT (Top View)

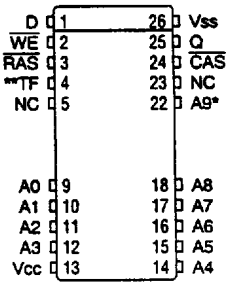
18-Pin DIP (DA-1)



20-Pin ZIP (DB-1)



20/26-Pin SOJ (DC-1)



*Address not used for $\overline{RAS}$ ONLY REFRESH
**TF = Test Function; V_{IN} must not exceed Vcc+1V for normal operation.

GENERAL DESCRIPTION

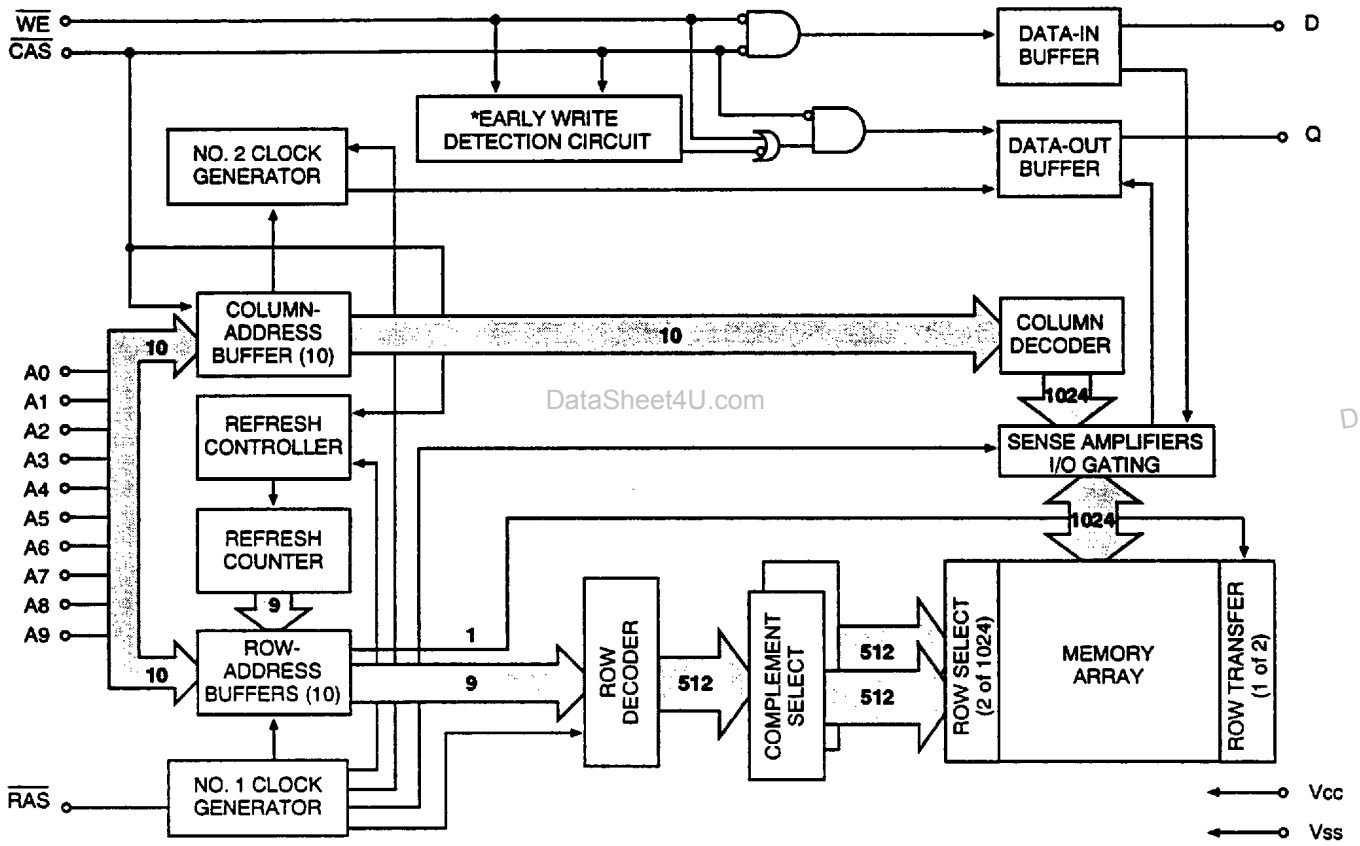
The MT4C1024(L) is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin, data-out (Q), remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and

strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms for the MT4C1024 or 64ms for the MT4C1024 L, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
LOW POWER, FAST PAGE MODE



***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA	
					^tR	^tC	D (Data-In)	Q (Data-Out)
Standby		H	H→X	X	X	X	"don't care"	High-Z
READ		L	L	H	ROW	COL	"don't care"	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In	High-Z
READ WRITE		L	L	H→L	ROW	COL	Data-In	Data-Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	"don't care"	Data-Out
READ	2nd Cycle	L	H→L	H	n/a	COL	"don't care"	Data-Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data-In	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data-In	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data-In	Data-Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data-In	Data-Out
RAS ONLY REFRESH		L	H	X	ROW	n/a	"don't care"	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	"don't care"	Data-Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data-In	High-Z
CBR REFRESH		H→L	L	X	X	X	"don't care"	High-Z
Extended Refresh (MT4C1024 L only)		H→L	L	X	X	X	"don't care"	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 600mW
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any inputs 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	VERSION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	MT4C1024	I_{CC2}	1	1	1	mA	
	MT4C1024 L	I_{CC2}	200	200	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: ^tRC = ^tRC [MIN])		I_{CC3}	90	80	70	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])		I_{CC4}	70	60	50	mA	3, 4, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])		I_{CC5}	90	80	70	mA	3, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC6}	90	80	70	mA	3, 5
REFRESH CURRENT: Extended Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) to1µs; $\overline{WE}$, A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (512 rows at 125µs = 64ms)	MT4C1024 L	I_{CC7}	200	200	200	µA	3, 5, 24

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5.0V ± 10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ WRITE cycle time	tRWC	135		155		175		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	60		65		70		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	tCAC		20		20		20	ns	15
Access time from column-address	tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time (CBR REFRESH)	tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	40	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row-address setup time	tASR	0		0		0		ns	
Row-address hold time	tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		0		ns	
Column-address hold time	tCAH	15		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	tAR	45		55		60		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	tOFF	3	20	3	20	3	20	ns	20, 25
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

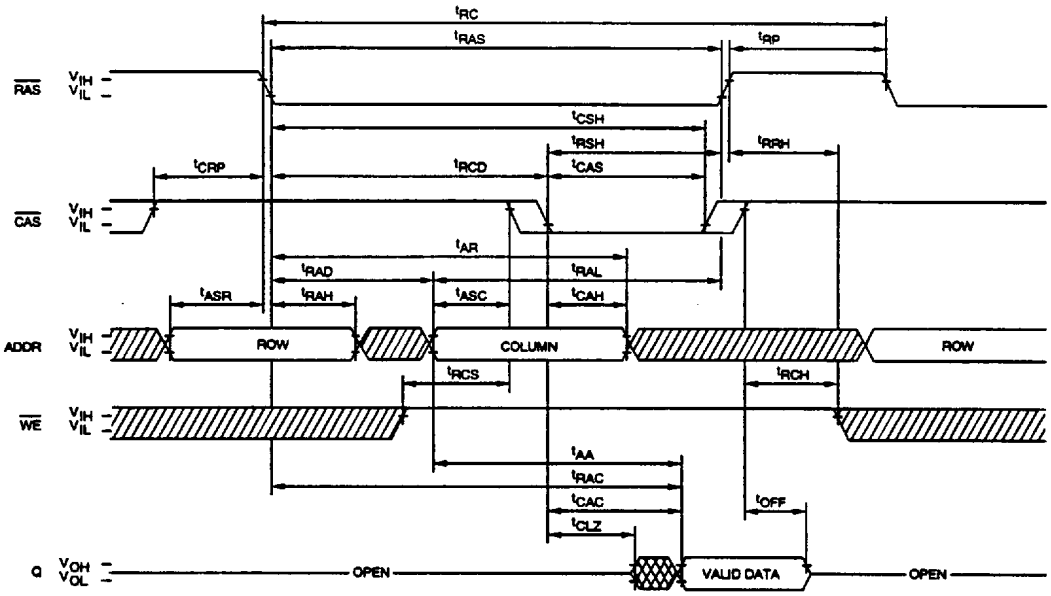
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	t_{WCR}	45		55		60		ns	
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		20		ns	
Data-in setup time	t_{DS}	0		0		0		ns	22
Data-in hold time	t_{DH}	15		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	t_{DHR}	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	60		70		80		ns	21
Column-address to $\overline{WE}$ delay time	t_{AWD}	30		35		40		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	15		20		20		ns	21
Transition time (rise or fall)	t_T	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles) MT4C1024 / MT4C1024 L	t_{REF}		8 / 64		8 / 64		8 / 64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	t_{CSR}	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	t_{CHR}	10		15		15		ns	5

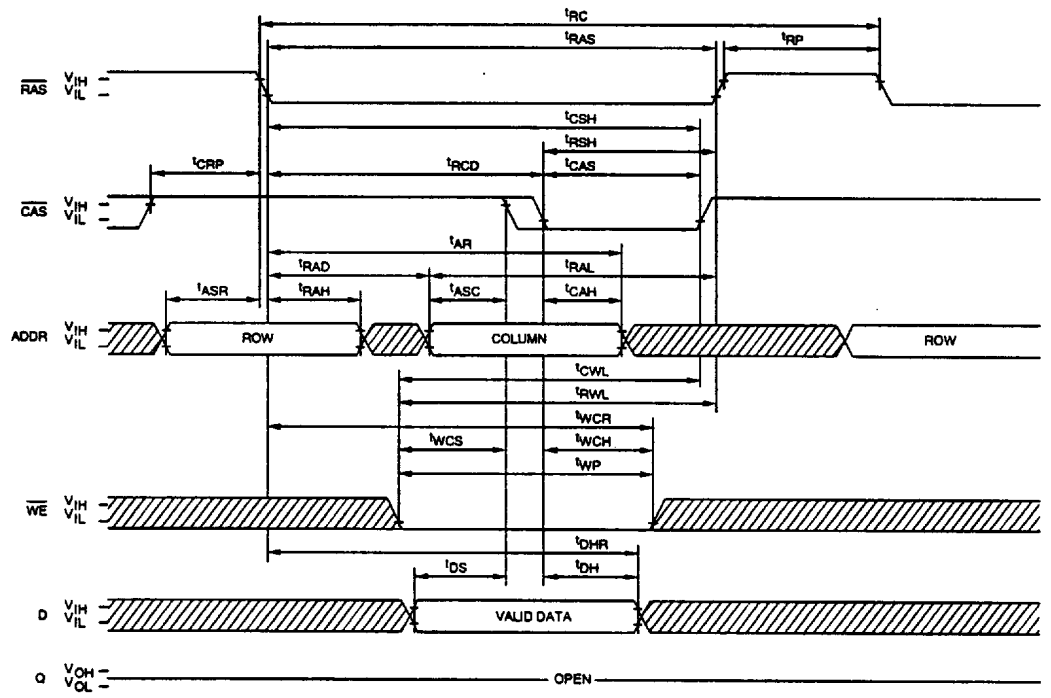
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE, and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE WRITE and the state of Q is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. Extended refresh current is reduced as ^{t}RAS is reduced from its maximum specification during the extended refresh cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.

READ CYCLE



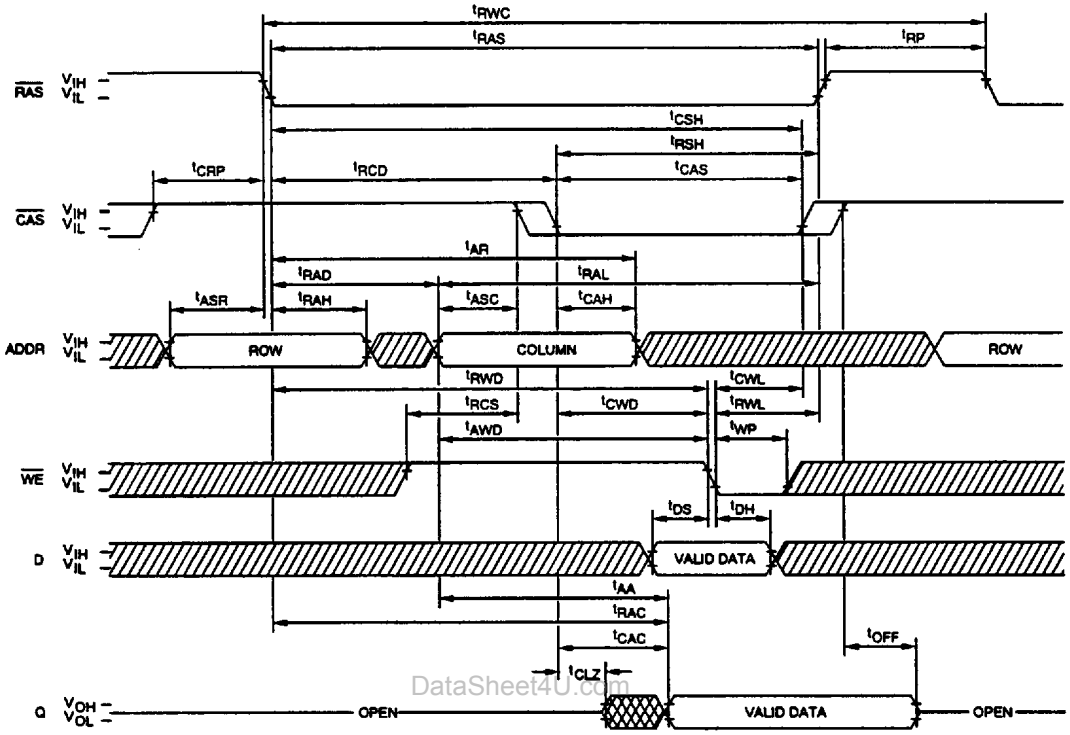
EARLY WRITE CYCLE



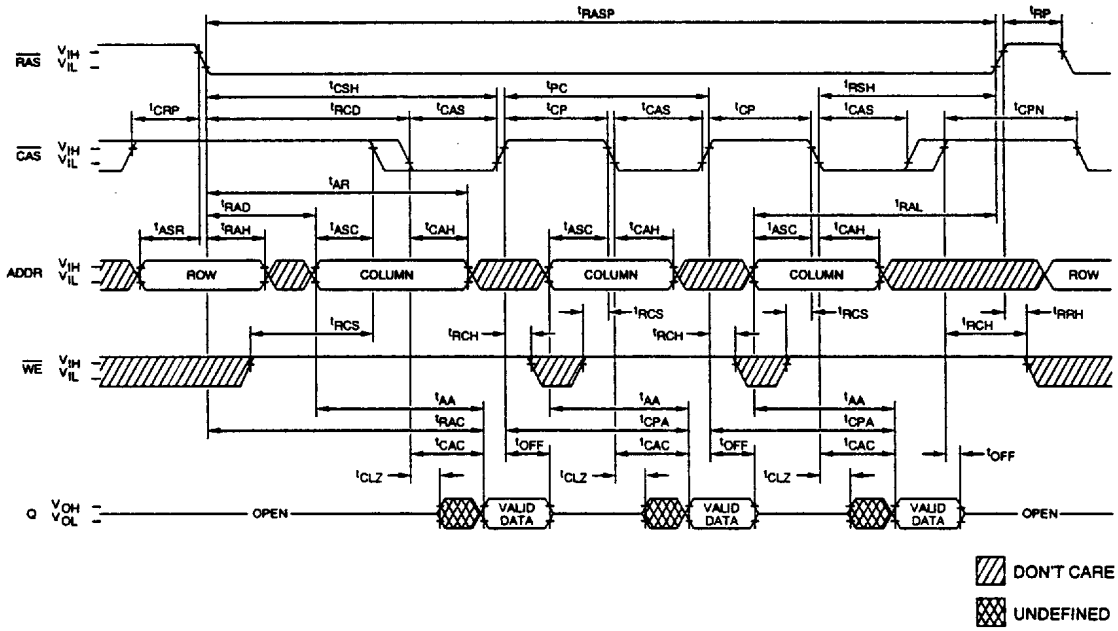
DON'T CARE

UNDEFINED

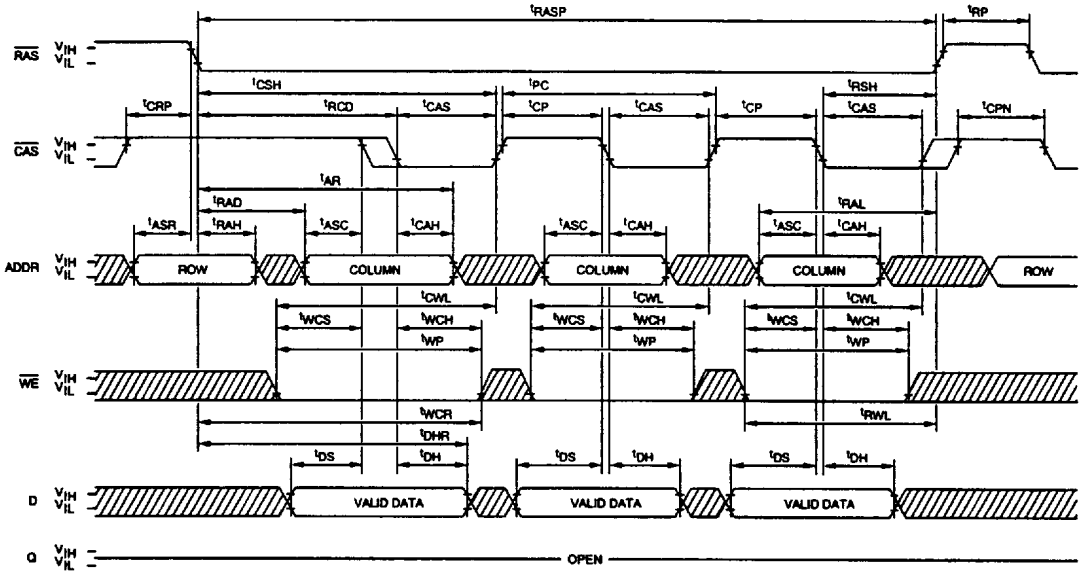
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



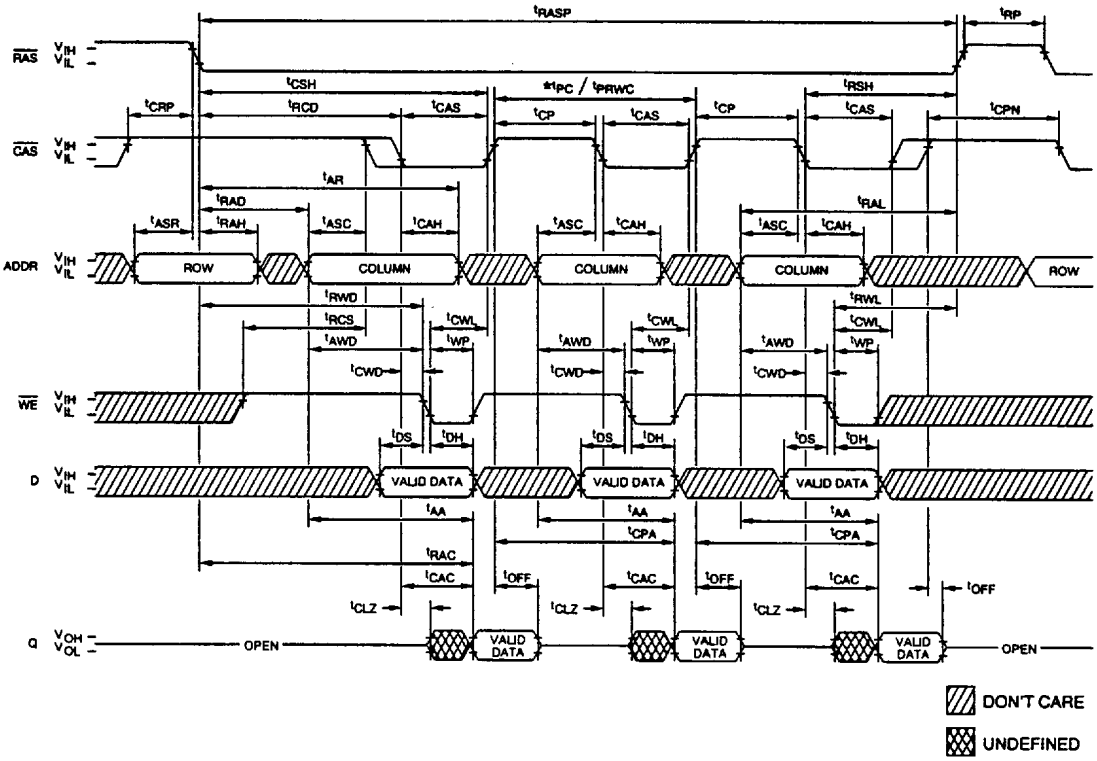
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

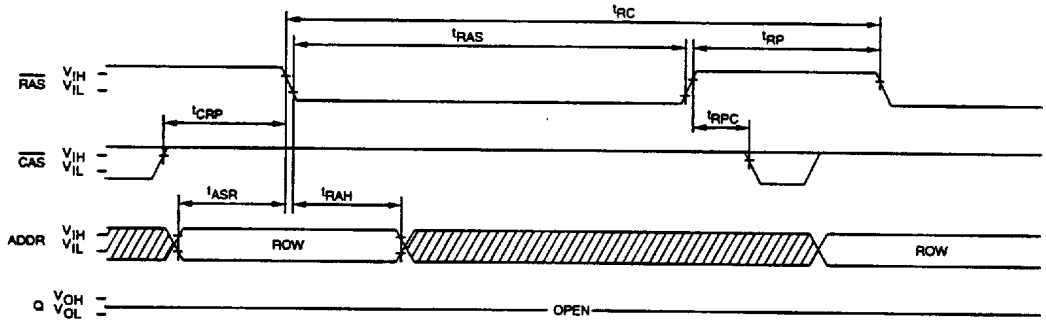


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)

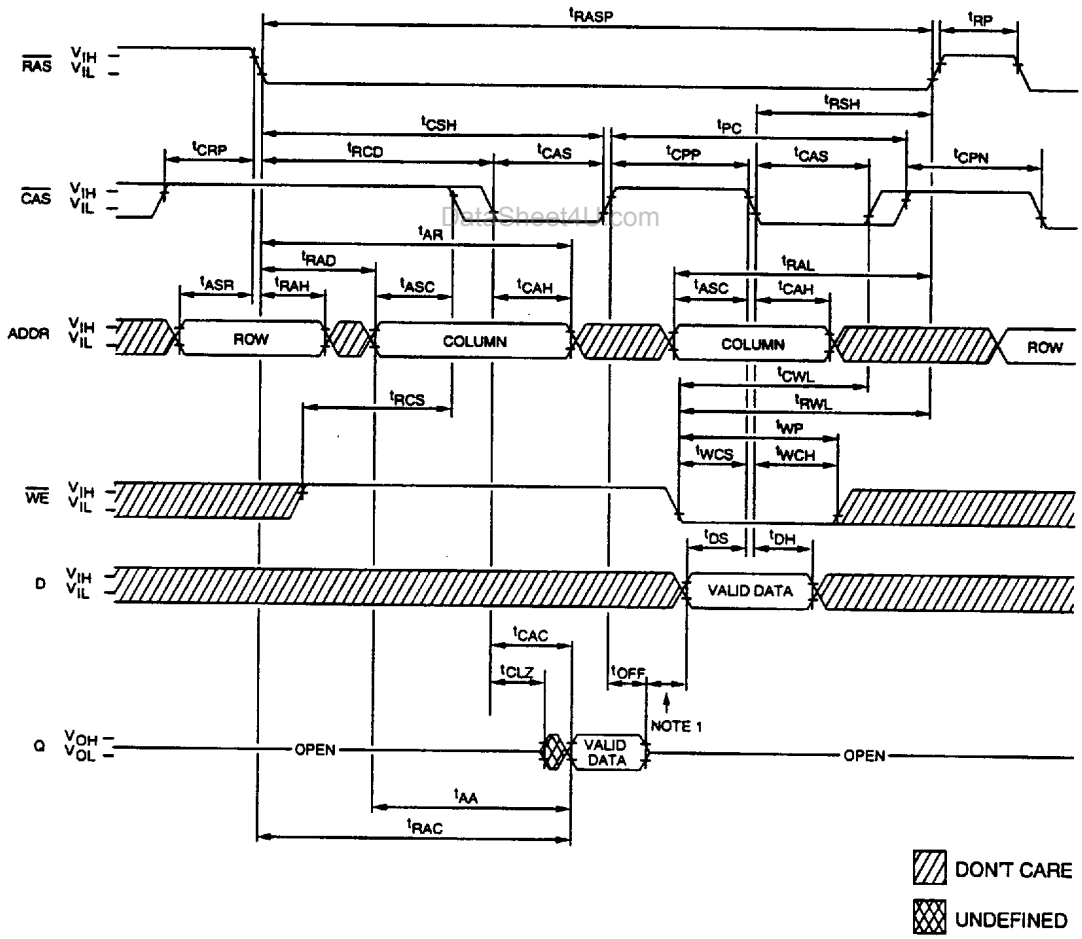


*tPC is for LATE WRITE only.

RAS ONLY REFRESH CYCLE
(ADDR = A0-A8; A9 and WE = DON'T CARE)

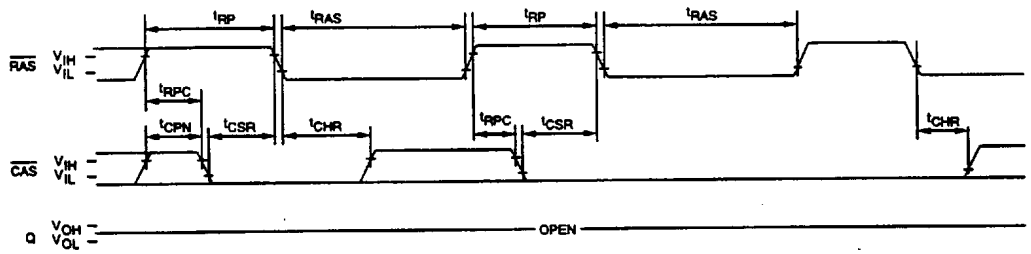


FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

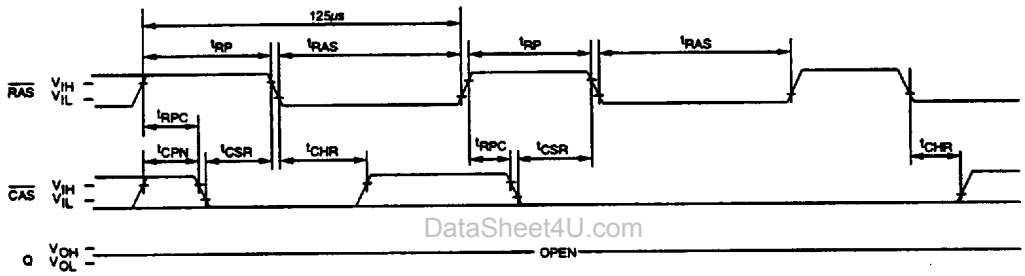


NOTE: 1. Do not drive data prior to tristate: ^tCPP(MIN) or ^tCP(whichever is greater) + ^tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

CBR REFRESH CYCLE
(A0-A9 and $\overline{WE}$ = DON'T CARE)



EXTENDED REFRESH CYCLE (MT4C1024 L ONLY)
(A0-A9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH)