DRAM MODULES

1MEG x 8 DRAM

FAST PAGE MODE

FEATURES

- Industry standard pin-out in a 30-pin single-in-line package.
- High performance CMOS silicon gate process.
- Single 5V±10% power supply.
- All inputs, outputs and clocks are fully TTL and CMOS compatible.
- Low power, 40mW standby, 1400mW active, typical.
- On-board power supply decoupling capacitors (0.2µf) for low noise.
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and Hidden.
- 512 cycle refresh distributed across 8ms.
- Optional Fast Page Mode.

OPTIONS MARKING

- Timing

80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15

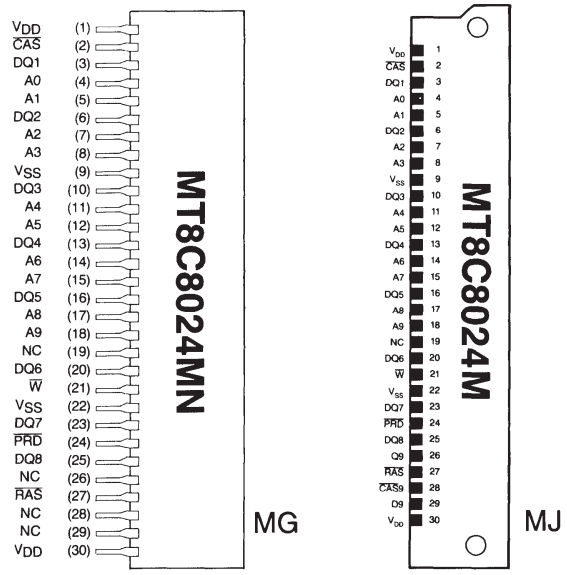
- Access Mode Option

Fast Page Mode	MT8C8024

- Packages:

Leadless 30-pin SIMM	M
Leaded 30-pin SIP	MN

PIN ASSIGNMENT (Top View)



A0-A9	Address Inputs	$\overline{CAS}$, $\overline{CAS9}$	Column Address Strobe
DQ1 - DQ8	Data-In/Data-Out	D9	Data-In
$\overline{PRD}$	Presence Detect	Q9	Data-Out
$\overline{RAS}$	Row Address Strobe	$\overline{W}$	Write Enable
VDD	Power (+5V)	Vss	Ground

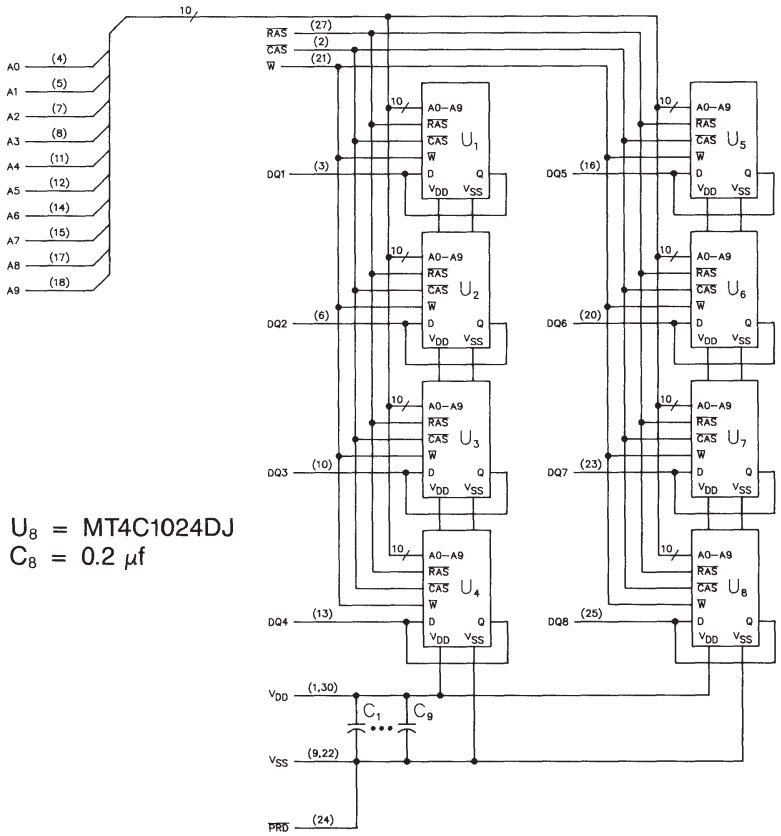
GENERAL DESCRIPTION

The MT8C8024M/MN is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x8 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic low on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (DIN) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, the output pin(s) remain open (High Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes low after data reaches the output pin(s), DOUT is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ low, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ high terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM



$U_1 - U_8$ = MT4C1024DJ
$C_1 - C_8$ = 0.2 µf

FUNCTIONAL TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 8 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$ = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		400	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		400	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		16	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		8	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		280	mA	3
REFRESH CURRENT: $\overline{CAS}$-before-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		280	mA	3, 5
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-80	80	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-80	80	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A_0-A_9)	C_{I1}		40	pF	18
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		56	pF	18
Output Capacitance D_{OUT}, D_{IN}	C_O		12	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	190		220		260		ns	
PAGE-MODE READ or WRITE cycle time	^tPC	55		70		85		ns	
Access time from $\overline{RAS}$	^tRAC		100		120		150	ns	14
Access time from $\overline{CAS}$	^tCAC		25		30		45	ns	15
Access time from column address	^tAA		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		50		65		75	ns	
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	100	100,000	120	100,000	150	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		30		45		ns	
$\overline{RAS}$ precharge time	^tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	25	10,000	30	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	15		20		25		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	10		15		20		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	75	15	90	15	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	10	50	15	60	15	70	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		80		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	50		60		70		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	5		5		5		ns	
Output buffer turn-off delay	^tOFF	0	25	0	25	0	30	ns	20
Write command hold time	^tWCH	20		25		30		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

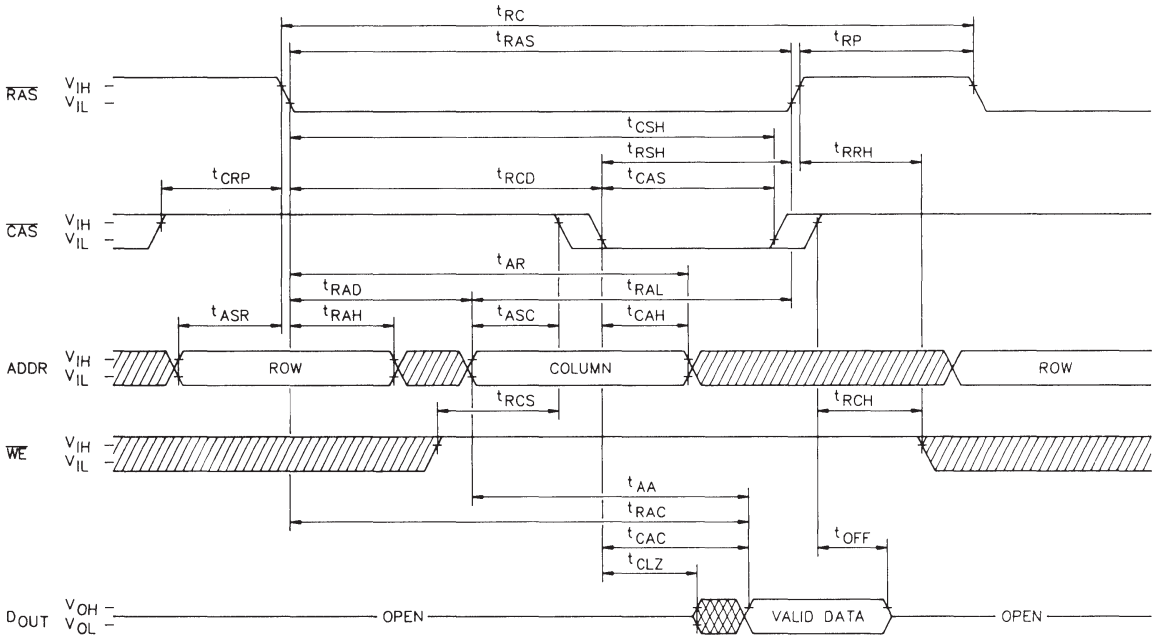
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	70		80		90		ns	
Write command pulse width	^tWP	20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	15		20		25		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		110		135		ns	
Column address to $\overline{WE}$ delay time	^tAWD	50		60		70		ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	35		40		45		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	5

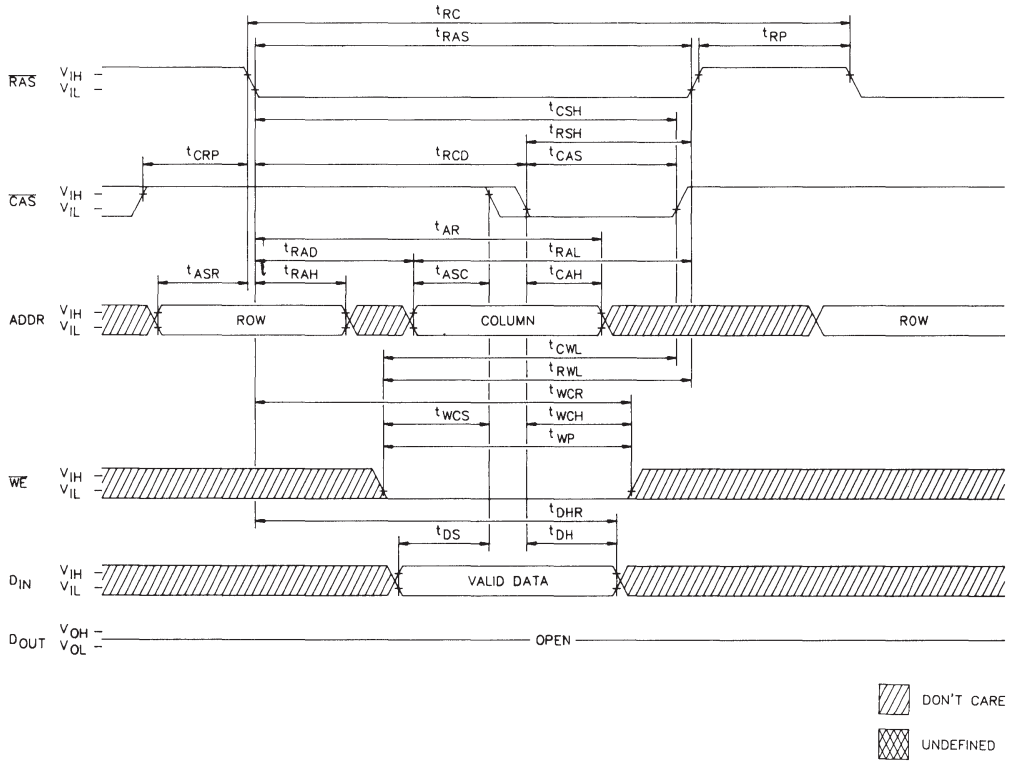
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} ot V_{OL}.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

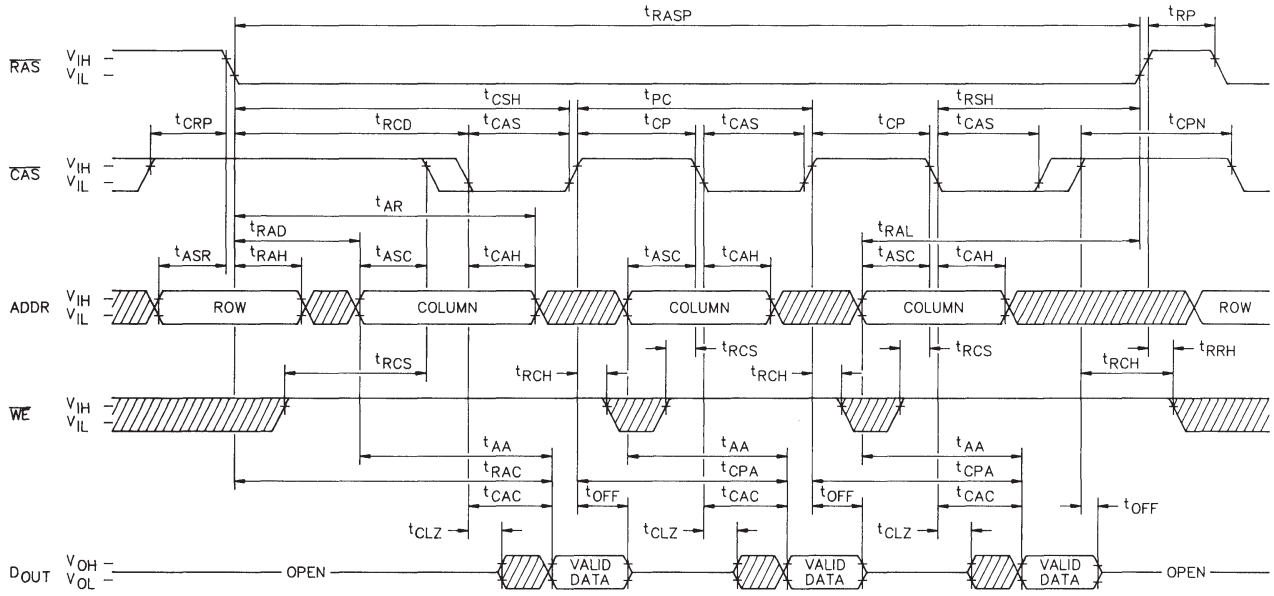
READ CYCLE



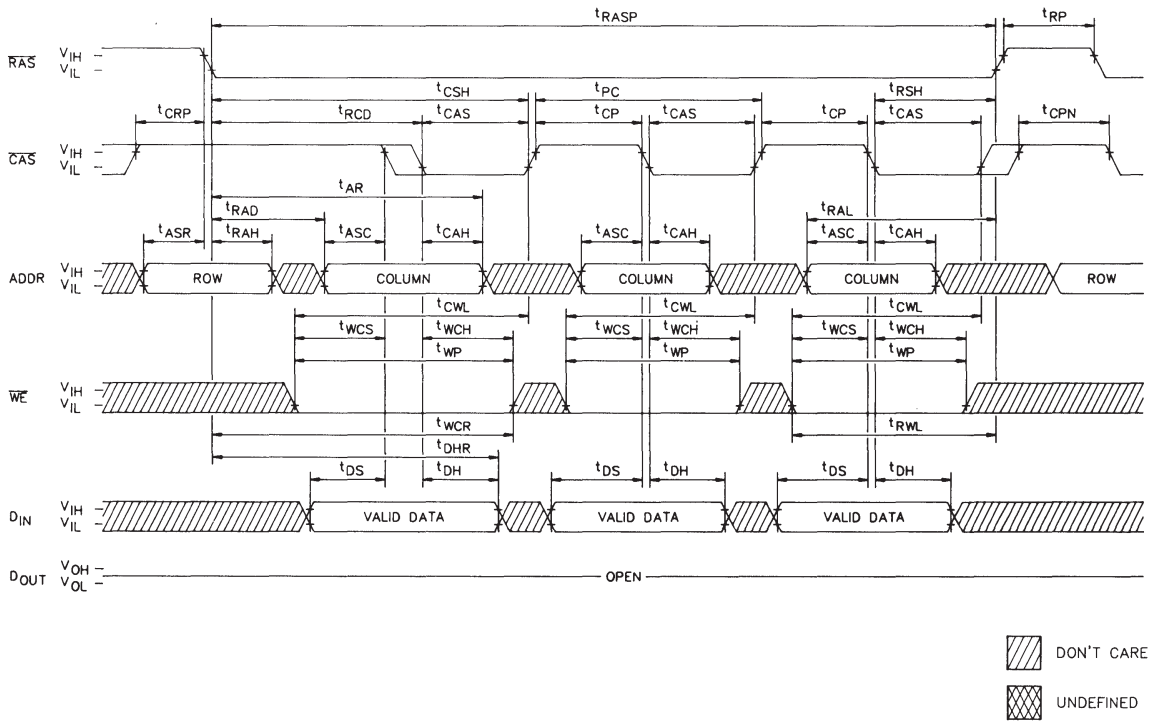
EARLY-WRITE CYCLE



PAGE-MODE READ CYCLE

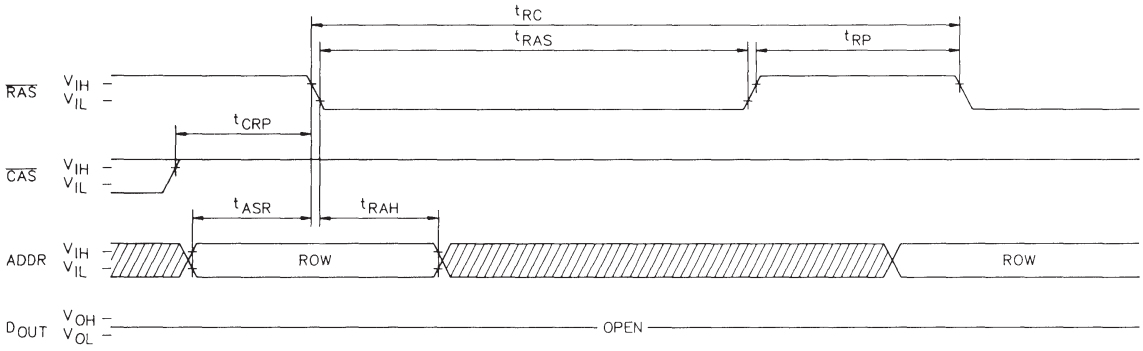


PAGE-MODE EARLY-WRITE CYCLE



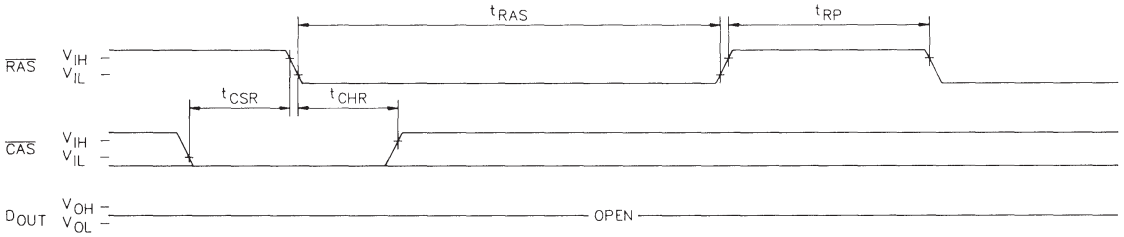
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



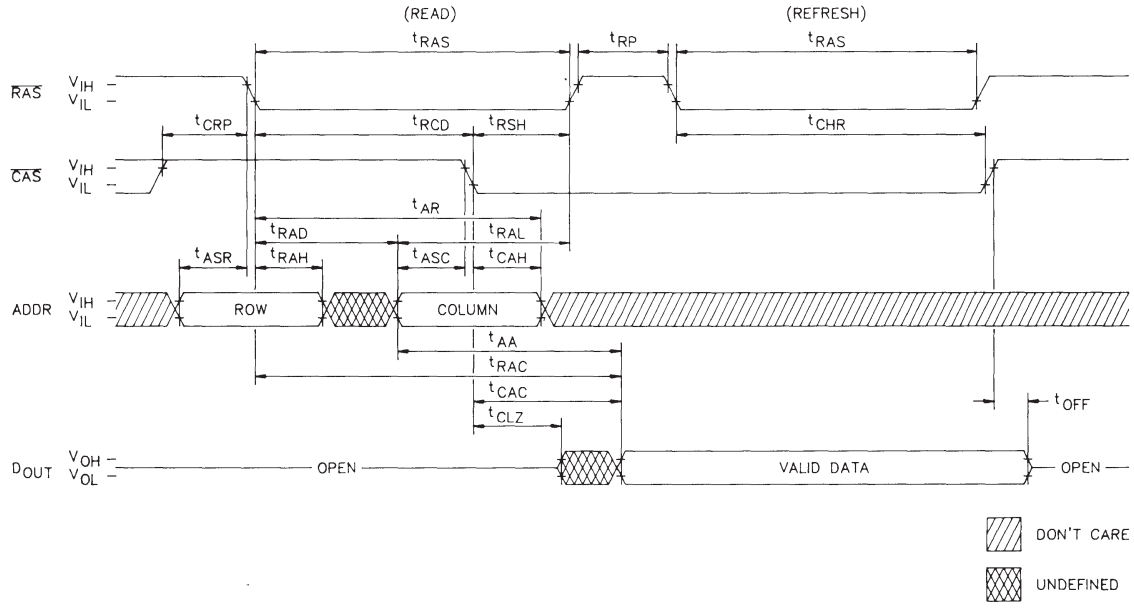
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 $\overline{WE}$, = DON'T CARE.)



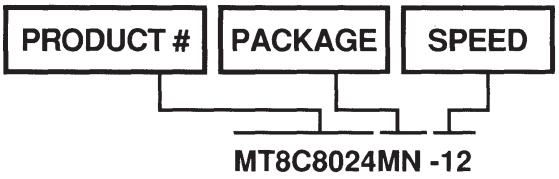
HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



ORDER INFORMATION

1 MEG x 8, 120ns access, Fast Page Mode Access, Leaded SIP



The Micron 1 MEG DRAM module family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacture's products meeting JEDEC standards. Several parameters are sampled; however, fuctionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring reliability and quality.