8. SYSTEM ENHANCEMENT MODULES

8.1 DCE-PWR : PLUG-IN POWER SUPPLY MODULE

8.1.1 FUNCTIONAL DESCRIPTION

The DCE-PWR is a regulated power supply module, which simply plugs into any standard DAI eurorack or eurobox. It operates from 220V or 110V A.C. input, and supplies the DCE-BUS power rails with regulated +5V, -5V and +12V D.C. The current outputs of 2.5A (+5V), 1A (-5 V) and 1A (+12V), are sufficient for DCE microcomputer systems with medium power requirements.

8.1.2 FEATURES

° Regulated plug-in power supply module.
° Plugs into any DAI eurobox or eurorack.
° Outputs of regulated +5V (2.5A), -5V (1A) and +12V (1A).
° 220V or 110V A.C. input.
° On/off switch and power-on LED indicator on front panel.
° Ripple less than 100 mV with severe dynamic load conditions.
° 3 mV typical ripple.

8.1.3 HARDWARE CONFIGURATION

The DCE-PWR module has an on/off switch and a power-on LED indicator on the front panel. All input and output connections are brought to 31-pin and 13-pin male connectors at the back of the module. These plug into corresponding female connectors on the DCE-BUS motherboard at the back of all standard DAI euroboxes and euroracks.

The pin definitions of these two male connectors are as follows:

31-pin connector	
pin	signal
1,2	-5V
3,4	+12V
5 → 28	GND
29 → 31	+5V

13-pin connector	
pin	signal
2	0V
6	110V
10	220V
13	GND

Mains power is derived via a separate Mains Power Adaptor module (PSM-MPA or PSM-MPA/C), which can be mounted at the front or back of the corresponding eurorack or eurobox. This MPA unit provides a mains power cable and connector, a power line noise filter, a fuse, an on/off switch, and an optional cooling fan (MPA/C). The power line noise filter provides approximately 30 dB attenuation for mains interference in the frequency range 600 Hz to 100 MHz.

An optional bench-top adaptor (PSM-PWR/B) is available for enclosing the DCE-PWR module and converting it to a bench-top version with 220V A.C. input. This adaptor provides an enclosure for plugging in the DCE-PWR module and has rubber feet, a fuse, a D.C. power output cable with a 4-pin connector and a mains cable.

8.1.4   ORDERING INFORMATION

DCE-PWR   : Standard version.

PSM-PWR/B   : The optional bench-top adaptor must be
                       ordered separately.

PSM-MPA/C, MPA : The mains power adaptor module, with or
                       without cooling fan, must be ordered
                       separately.

8.2   DCE-PWR/H : HEAVY-DUTY PLUG-IN POWER SUPPLY MODULE

8.2.1   FUNCTIONAL DESCRIPTION

The DCE-PWR/H is a heavy-duty regulated power supply module, which simply plugs into any standard DAI eurorack or eurobox. Because of its extra width it occupies more space than the DCE-PWR module when plugged in, and covers one extra card guide adjacent to it. It operates from 220V or 110V A.C. input, and supplies the DCE-BUS power rails with regulated +5V, -5V and +12V. The current outputs of 10A (+5V), 2A (-5V) and 2A (+12V) are sufficient for powering all DCE microcomputer configurations, including the diskette system.

The module contains an over-heating cut-out, which will cause all the power outputs to be switched off automatically if over-heating occurs for any reason. If any of the three output voltages rise above specified limits, an over-voltage protection feature will blow the fuse and switch off all outputs.

The module continuously monitors the A.C. mains supply, and the absence of a half-cycle produces a mains failing signal, which can be used to implement an automatic 24V battery back-up feature.

8.2.2   FEATURES

° Heavy-duty regulated plug-in power module.

° Plugs into any standard DAI eurobox or eurorack.

° Outputs of regulated +5V (10A), -5V (2A) and +12V (2A).

° Over-heating and over-voltage protection.

° 110V and 220V A.C. inputs.

° Ripple less then 200 mV under full load.

° Mains power failing signal, and 24V battery back-up capability.

8.2.3   <u>HARDWARE CONFIGURATION</u>

The DCE-PWR/H module is based on a switching type design
giving a higher efficiency than the conventional types. It contains
an over-heating cut-out, which will cause all the power outputs
to be switched off automatically if over-heating occurs for any
reason. The over-heating cut-out will switch off the power
outputs without blowing the fuse. After such a cut-out, the power
supply must be disconnected from the mains and left to cool
before it can function again.

If any of the three output voltages rise above specified limits, an
over-voltage protection feature will switch off all outputs by
blowing the fuse. The over-voltage protection feature is triggered
at the following approximate levels:

+5V   :   5.8V
-5V   :   1.4V
+12V :   12.7V

A LED indicator on the front panel of the module provides a
visual indication of active mains or battery power input.

The power supply module continuously monitors the A.C. mains
supply, and the absence of a half-cycle causes a logic 1 to appear
on the "Mains Failing" signal at pin 13 of the 31-pin connector.
During normal operation this signal is at logic 0. This signal
is not latched, and therefore a logic 1 appears on it only during
the time that the half cycles of the mains supply are not being
detected. This Mains Failing signal can be used to implement
an automatic switch-over to an external 24V battery, to ensure
system operation without interruption.

All input and output connections are brought to 21-pin and 31-pin male connectors at the back of the module. These plug into corresponding female connectors on the DCE-BUS motherboard at the back of all standard DAI euroboxes and euroracks.

The pin definitions of these two male connectors are as follows:

31-pin connector		21-pin connector	
pin	signal	pin	signal
1,2	-5V	8	0V
3,4	+12V	12	110V
5 → 8	GND	16	220V
9 → 12	24V battery input	19	GND
13	Mains Failing		
28 → 31	+5V		

Mains power is derived via a separate Mains Power Adaptor module (PSM-MPA or PSM-MPA/C), which can be mounted at the front or back of the corresponding eurorack or eurobox. This MPA unit provides a mains power cable and connector, a power line noise filter, a fuse, an on/off switch, and an optional cooling fan (MPA/C). The power line noise filter provides approximately 30 dB attenuation for mains interference in the frequency range 600 Hz to 100 MHz. A separate PSM-MPA/B module, very similar to PSM-MPA/C, provides additional connections to a 24V battery and a trickle charging supply. Another separate module, PSM-BAT, provides a 24V 1.8 Ah battery with trickle-charge circuitry on a panel, for mounting on the back of a large eurorack or eurobox in place of the PSM-PCP/L cover panel.

8.2.4   ORDERING INFORMATION

DCE-PWR/H   : Standard version.

PSM-MPA, MPA/B, MPA/C   : The mains power adaptor
                                       module, with or without
                                       the battery back-up and
                                       cooling fan options, must
                                       be ordered separately.

PSM-BAT   : The optional back-up
                                       battery module must be
                                       ordered separately.

8.3   DCE-PRG : EPROM PROGRAMMER MODULES

8.3.1   FUNCTIONAL DESCRIPTION

The DCE-PRG/8 and DCE-PRG/16 modules provide all the necessary
hardware functions for programming and accessing 2708 or 2716
EPROMs under DCE control.   Each module has a zero-insertion-
force socket for easy insertion of EPROMs.   A programming
disable switch on the module prevents accidental alteration of
EPROM contents while in the socket.   A LED lamp provides a
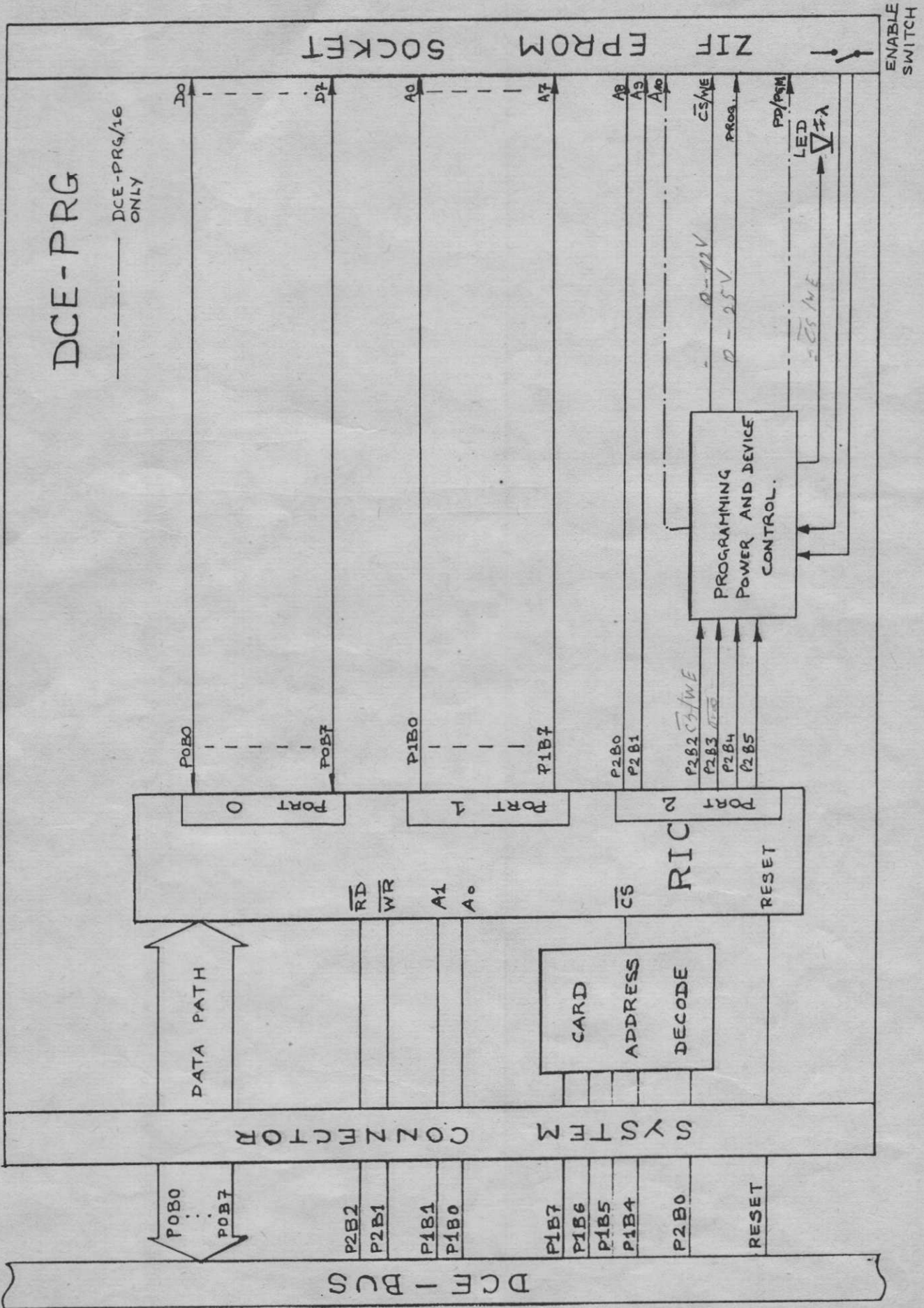visual indication of when a programming operation is in progress.

All DCE microcomputer Utility software packages contain routines
for driving the corresponding versions of DCE-PRG modules.   A
Programming function enables the contents of any DCE system
memory block to be transferred to one or more locations of an
erased EPROM in the socket.   After programming, the new contents
of the EPROM locations are automatically compared with the
corresponding memory contents, and any discrepancies reported.
Utility commands can be used to compare contents of selected
locations of an EPROM with memory, and to transfer selected
locations to system RAM memory.

Each card has an identification address defined by a hexadecimal
switch, and up to fifteen can be directly connected to the DCE-BUS.
This feature enables several DCE-PRG modules to be configured
together for programming several EPROMs simultaneously.

8.3.2   FEATURES:

   ° Programs 2708, or 2716 EPROMs under DCE microcomputer
     control.

   ° LED lamp for visual indication of programming operation.

   ° Programming disable switch prevents accidental alteration of
     EPROM contents.

8.3.3 FUNCTIONAL BLOCK DIAGRAM

DCE-PRG

DCE-PRG/16 ONLY

ZIF EPROM SOCKET

ENABLE SWITCH

D0 ─── D7 A0 ─── A7 A8 A9 A10 CS/WE PROG. PD/PGM LED

0 - 12V
0 - 25V
~CS/WE

PROGRAMMING POWER AND DEVICE CONTROL.

POB0 ─── POB7   P1B0 ─── P1B7   P2B0 P2B1   P2B2 CS/WE P2B3 PROG P2B4 PD P2B5

PORT 0   PORT 1   PORT 2

RIC

RD WR A1 A0 CS RESET

DATA PATH

CARD ADDRESS DECODE

SYSTEM CONNECTOR

POB0 ... POB7   P2B2 P2B1   P1B1 P1B0   P1B7 P1B6 P1B5 P1B4   P2B0   RESET

DCE - BUS

° Includes zero-insertion-force EPROM socket.

° Uses standard DCE-BUS power supplies.

° Standard hardware and software interface to the DCE-BUS.

° Switch selectable module address.

° Single 100 x 160 mm eurocard format.

8.3.4   SYSTEM DESIGN PARAMETERS

8.3.4.1   Hardware Configuration

The functional block diagram given in section 8.3.3 illustrates the hardware configuration of the DCE-PRG module. It has the standard RIC interface to the DCE-BUS.

PORT 1 of the RIC and two (or three) lines of PORT 2 are used to address the EPROM contents. PORT 0 is used to transfer data both to and from the EPROM. A Hexadecimal switch allows the module card address to be configured. Thus, multiple EPROM programming modules can be independently accessed.

8.3.4.2   Programming Specifications

The DCE-PRG is addressed via the DCE-BUS via the standard DCE-BUS interface (see section 4.1 of this manual).

DAI System software assumes the card addresses as follows:

2704/2708	DCE-PRG/8	ADDRESS = 'F'
2516	DCE-PRG/16	ADDRESS = 'B'

The timing requirements of the programming process are controlled by the system CPU. Suitable drive software is included in DAI's UTILITY and REAL-WORLD BASIC programs, versions of which exist for either 2708 or 2716 device programming.

out ПF3, П90   init
out ПF1, AD 1AND FF
out ПF2, AD SHR 8 1AND 7

$M = INP(ПF1)$

Reading data from an EPROM inserted into the DCE-PRG module
can be achieved by initialising the RIC with control word 90H.
Thereafter, any address written to RIC port 1, and bits 0, 1 and
2 of port 2, can be read directly on RIC port 0. All other bits
on port 2 shall be set to 0.

out ПF3, П80
out RF0, DATA
out ПF1, AD 1AND FF
out ПF2, AD SHR 8 1AND 7

Programming is enabled by setting the program-switch up.
The RIC shall be initialised with control-word 80H. Then, for
each byte set on RIC port 0, the required address is set on port
1 and 2 (as above) with the port 2 data merged with either 0CH
(for DCE-PRG/8) or 20H (for DCE-PRG/16). The programming
pulse is then given by using the RIC bit-set and bit-clear facility.
P2 B2 is pulsed low on the DCE-PRG/8. For the DCE-PRG/16
module, P2 B3 is pulsed high.

The user must never insert or remove the EPROM whilst the
device is selected for programming. After the programming
cycle is complete, initialisation of the module to read (control
word 90H) will extinguish the indicator LED.

8.3.4.3   Operational Requirements

Signal characteristics.

When operated by the standard DAI programming software, the
DCE-PRG modules provide an approved EPROM programming
facility. All signal levels and timing are according to the
specified programming conditions provided by the device
manufacturer.

(A) 1 program pulse length $0,1 ms < T_{PPL} < 1 ms$

(B) Total programming time $\geq 100 ms$

$\Rightarrow$ Number of loops $= \dfrac{100 ms}{T_{PPL}} = N$

DATPC: $T_{PPL} \approx 1 mA$

EPROM types

All versions of the 2708, 8708, 2704 family of EPROMs may be programmed with the DCE-PRG/8.

Note: Only single +5V supply EPROMs may be programmed with the DCE-PRG/16. Earlier 3 supply devices (e. g. TMS-2716) should not be used with this programmer module.

Power Requirements

The DCE-PRG card uses all 3 DCE-BUS supply lines. Typical power consumption from each, under programming conditions, are:

PRG/8: +5V   120 mA   PRG/16: +5V   175 mA
       +12V   75 mA   +12V   85 mA
       -5V   50 mA   -5V   50 mA

Environmental Requirements

Operating temperature	: 0°C to 55°C
Storage temperature	: -25°C to 85°C
Relative humidity	: 95 % non-condensing

Bus Loading

The RWC-PRG module presents 1 unit-load to the DCE-BUS (see Section 4. 4).

8. 3. 5   ORDERING INFORMATION:

DCE-PRG/8   : Standard version for 1K byte 2708 EPROMs.
DCE-PRG/16   : Standard version for 2K byte 2716 EPROMs.

8.4   DCE-SBM : SYSTEM BUS MONITOR

8.4.1   FUNCTIONAL DESCRIPTION:

The DCE-SBM System Bus Monitor module provides 24 LED
indicator lamps for monitoring the status of the address, data
and control lines of the DCE-BUS. 24 switches, also connected
to the DCE-BUS lines, enable manual generation of input signals
to the bus. A system Reset switch enables the entire DCE
microcomputer system including RWC Real-World interface
modules to be reset. Two jumper contacts allow manual
generation of the two interrupt request signals carried by the
DCE-BUS.

The 24 LED indicators are arranged as two groups of eight and
two groups of four, to match the organisation of the three
programmable ports of the DCE microcomputers. Similarly,
the 24 switches are arranged as three groups of eight. When the
DCE microcomputer is used as a stand-alone controller, the DCE-
SBM can be used during the software development phase to simulate
data inputs, and monitor signal outputs. It can also be used to drive
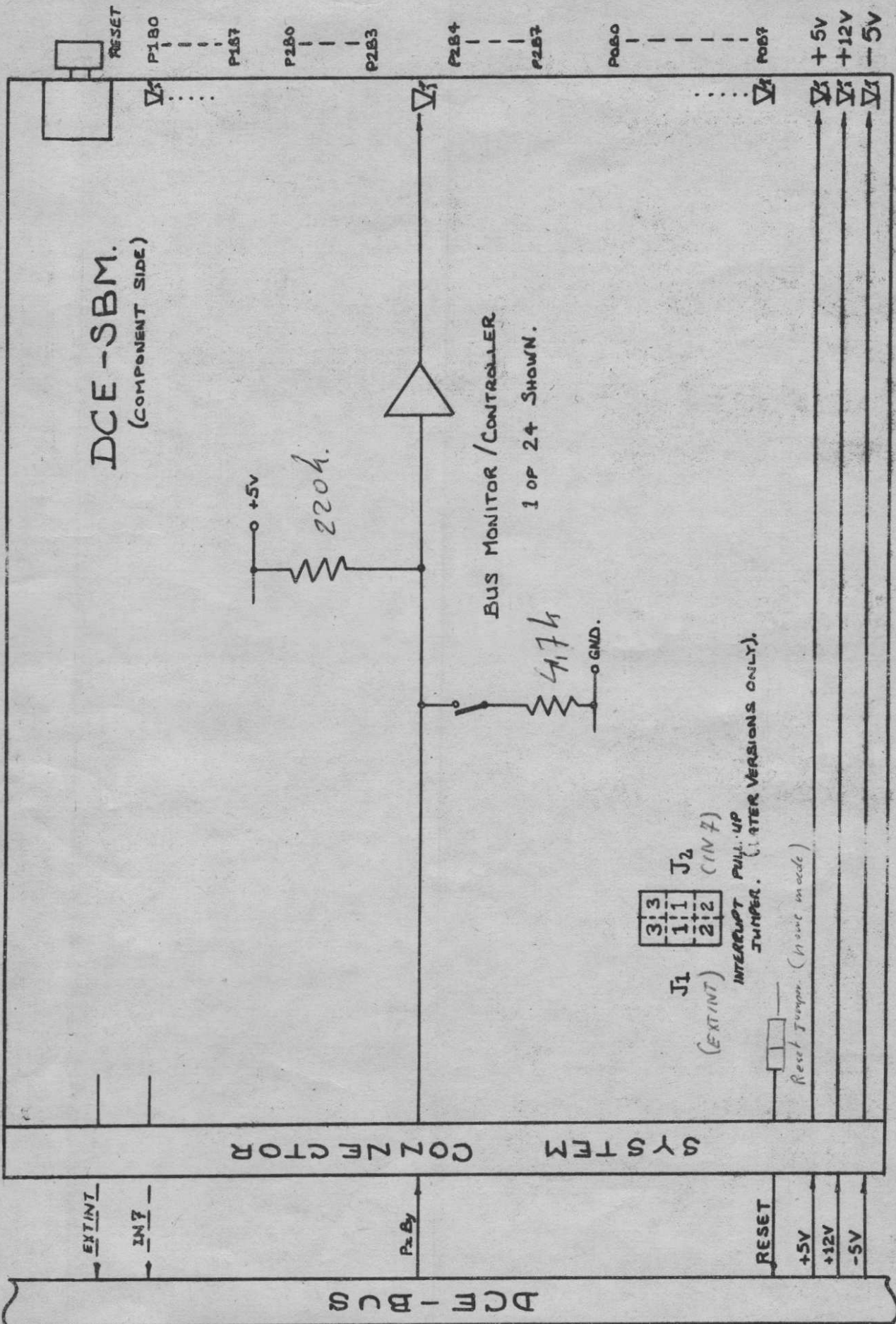RWC interface modules manually for testing purposes.

The Reset switch and the LED indicators are mounted at the front
edge of the module, for ease of access when plugged into a system.
In order to make the switches accessible, the module should be
inserted into the eurobox or eurorack, via a DCE-EX extender card.
All the circuitry of the DCE-SBM module will then be completely
accessible.
Later versions of the DCE-SBM also include LED indicators for
each of the three system power supply rails.

8.4.2   <u>FEATURES</u>:

° 24 LED indicator lamps displaying the status of DCE-BUS lines.

° 24 switches for manual input of signals to the DCE-BUS lines.

° System Reset switch.

° Jumper contacts for manual generation of the two DCE-BUS interrupt request signals.

° Single 100 x 160 mm eurocard format.

). 4. 3.   FUNCTIONAL BLOCK DIAGRAM

DCE - SBM.
(COMPONENT SIDE)

RESET

P1B0 - - - - - P1B7   P2B0 - - - - P2B3   P2B4 - - - - P2B7   P6B0 - - - - P6B7

+5V

$220\,\Omega$.

BUS MONITOR / CONTROLLER
1 OF 24 SHOWN.

$4.7\,k$

GND.

J1   J2
(EXTINT)   (IN 7)

3	3
1	1
2	2

INTERRUPT PULL-UP
JUMPER. (LATER VERSIONS ONLY).

Reset Jumper. (move mode).

+5V
+12V
-5V

POWER STATUS.
(LATER VERSIONS ONLY.)

SYSTEM CONNECTOR

EXTINT
IN 7

P6 B7

RESET

+5V
+12V
-5V

DCE - BUS

8.4.4 SYSTEM DESIGN PARAMETERS

8.4.4.1 Hardware Configuration

The DCE-SBM provides LED indicators of the DCE-BUS. The
status of DCE-lines, normally driven by the three ports of the
GIC, are given by a correspondance of: 0 = LED off; 1 = LED on.

The module also provides 24 switches, arranged as three banks
of eight. The switches can be used to drive the 24 lines of the
DCE-BUS for manually performing data transactions to and from
any DCE-BUS compatible module.

A pushbutton switch is also provided on the DCE-SBM module.
This is connected to the system reset line of the DCE-BUS.
Activation of this push-button will cause a hardware reset of the
DCE microcomputer, and also of any Real-World cards that are
connected to the reset line. Thus, all RIC devices are configured
as read ports, etc.

Later versions of the DCE-SBM module also provide the following
additional features:
Firstly, all three DCE power supplies are monitored, and their
presence is shown by three status LEDs provided for this purpose.
Secondly, a pull-up or pull-down feature can be selected by
positioning a small movable jumper. One is provided for each
system interrupt line. J1 controls the EXTINT line, whilst J2
controls IN7. Configuration by each is as follows:

      Pull-up: Link 1 and 3
      Pull-down: Link 1 and 2

The module is supplied with the jumpers positioned to affect a
pull-down function.

Use of the switches provided on the DCE-SBM module.

The switches can be used to manually set up addresses on the DCE-BUS. They can also be used to generate the other signals necessary to affect a communication of data over the DCE-BUS. Each switch corresponds directly with each of the 24 data LEDs provided on the module when the lines are in input mode.

Driving a DCE-BUS line by switch on DCE-SBM

There are 24 switches available for driving the 24 lines of the DCE-BUS. If a particular switch is required to drive any DCE-BUS line, any other device connected to the same line must be operating as an input. (If a device is currently driving the line, the operation of the switch will have no effect). In this way the status of a DCE-BUS line is determined by its respective switch as follows:

switch closed: line pulled to logic '0'
switch open: line pulled to logic '1'

The LEDs indicate the status of the line as usual.
If a particular switch is not used for determining the status of a DCE-BUS line, it must be placed in its 'OPEN' position.
Whenever the DCE-SBM module is only used for monitoring the DCE-BUS, all 24 switches must be in their OPEN positions.

8. 4. 4.2 Operational Requirements

DCE-BUS Loading

DCE-BUS	Switch Status	Current
0	OPEN	: 50 µA
1		: 10 µA
0	CLOSED	: 50 µA
1		: 1 mA

Power Requirements

+5V   : 280 mA, all LEDs on.

+12V   : 20 mA

-5V   : 20 mA

Environmental Requirements

Operating temperature	: 0°C to 55°C
Storage temperature	: -25°C to +85°C
Relative humidity	: 95 % non-condensing

Bus Loading

The DCE-SBM module presents 1 unit-load to the DCE-BUS (see section 4. 4).   All switches are open.

8. 4. 5   ORDERING INFORMATION

DCE-SBM	: Standard version.
DCE-EX	: Extender card must be ordered separately.

8. 5   PDM-KDU : HAND-HELD KEYBOARD/DISPLAY UNIT

8. 5. 1   FUNCTIONAL DESCRIPTION

The PDM-KDU is a very low-cost alternative to a teletype or a
terminal for interacting with DCE microcomputer systems. It is
provided with a connecting cable, and can be plugged directly into
the TICC parallel ports of the DCE microcomputer via the device
connector.

The PDM-KDU driver Utility program UPK provides the following
functions and facilities: system initialization, display/modify
memory locations and CPU registers, move and fill memory blocks,
set-up or change the RAM vector addresses of interrupt service
routines, initiate program execution, single-step and trace program
execution and program EPROMs including compare-with-memory
and transfer-to-memory functions. The PDM-KDU provides all
necessary functions for program modification in the field. Only an
EPROM programmer card is necessary for transferring the
modified program on to EPROMs.

8. 5. 2   FEATURES

° Hand-held keyboard/display terminal for DCE microcomputer
  systems.

° 23 push switches for hexadecimal data and function input.

° 7-segment LED display for 9 hexadecimal digits.

° 5 modes of operation: Register, Memory, Vector, Function,
  Compare.

° 5 LEDs for indicating the current mode of operation.

° EPROM programming functions: Program, Transfer, Compare.

° Utility functions: Zero and initialize, Move, Look, Fill.

° Program debug functions: enter program, single-step and
  program trace.

° Display or modify DCE memory and CPU registers.

° Direct interface to DCE microcomputers via TICC parallel ports.

8.5.3   FUNCTIONAL BLOCK DIAGRAM
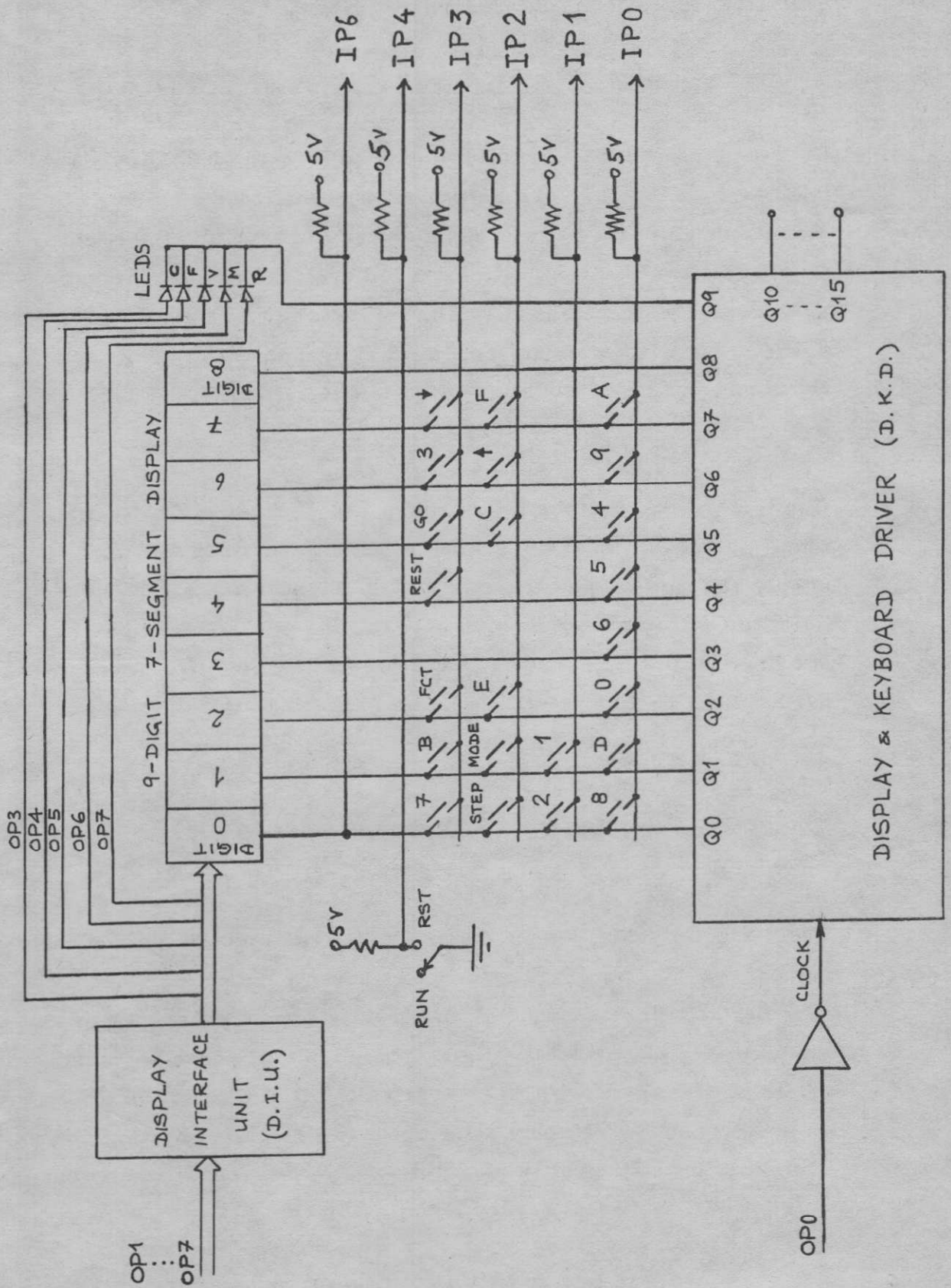
8.5.4   SYSTEM DESIGN PARAMETERS

8.5.4.1   Hardware Configuration

Section 8.5.3 shows a functional block diagram of the Keyboard
Display Unit (KDU).   The KDU houses twenty four switches.
Twenty three of these switches are Key pad type and the twenty
fourth is a two position switch.   The keys in the block diagram
are marked with the same symbols as on the front plate of the
KDU.   The KDU also houses a 9-digit 7-segment display, and
five light emitting diodes indicated by the symbols C, F, V, M,
R.

Communication with the KDU is done via 16 lines.   Fourteen of
these lines are signal lines, and the other two lines are used to
supply +5V and 0V power to the KDU.   Eight of the signal lines
(OP0 to OP7) are used to send data to the KDU.   The remaining
six lines (IP0 to IP4 and IP6) are used to receive data from the
KDU.   This 16-line interface enables the nine-digit display to be
activated, any or all of the five LEDs to be illuminated, and all
the switches to be monitored.

9-digit Display

The 9-digit display is used dynamically, and must be periodically
refreshed.   Each digit is made up of seven segments.   The
'Display Interface Unit' (D.I.U.) directly drives all anodes of all
the digits.   The particular digit of the display, whose segments
are to be illuminated by the data from the D.I.U. is selected by
a signal from the 'Display and Keyboard Driver' (D.K.D).   The
D.K.D. allows current to pass through to the cathode of any one
of the digits or LEDs thereby illuminating it.

Signal lines OP1 to OP7 drive the D. I. U, whose input requirements
are those of TTL. They drive the anodes of the five LEDs and of
the segments in the selected digit. Table 8. 5. 1 indicates the
relationship between these signal lines, the anodes of the LEDs,
and the anodes in the segments of the digit selected by the D. K. D.

The D. K. D. is used to select the cathodes of the required digit or
LED to be activated at any given time. The D. K. D. is a dynamic
device and needs a clocking signal. Signal line OP0 is used for
this. The requirements of OP0 are those of TTL. The D. K. D.
essentially comprises a 16-stage counter with 16 output lines Q0
to Q15. Eight of these output lines are used to select the cathodes
of the digit display. The required cathode to be activated is chosen
by clocking the D. K. D. an appropriate number of times. A high
going edge on OP0 is used to provide the clock. The D. K. D. has
an automatic time-out of 7. 5 msecs. This means that if clock
pulses are not provided every 7. 5 msecs, the 9-digit display and
the LEDs are deactivated and none of the cathodes are allowed to
sink current. In this condition the 16-bit counter within the D. K. D.
is set to count 15. This condition remains until the arrival of the
next clock pulse.

The counter within the D. K. D. unit counts from 0 to 15 and activates
outputs Q0 to Q15 sequentially (active low). Each clock pulse
increments its count by one and activates the next output line.
When at count 15, a further clock puts it back to count 0. To
activate the cathode of digit "i" requires the counter within the
D. K. D. to be clocked to count "i" (0 to 8). The KDU allows the
monitoring of the state of the counter within the D. K. D. The signal
line IP6 is used for this. This signal is TTL compatible. A logic
'0' on this line indicates that the D. K. D. counter is at value 0.

```
      A
   ┌───────┐
 F │   G   │ B
   ├───────┤
 E │       │ C
   └───────┘
      D
```
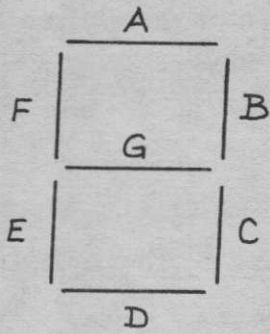
Segment in selected digit	Anode drive Signal	LED whose anode is driven
A	OP7	R
B	OP6	M
C	OP5	V
D	OP4	F
E	OP3	C
F	OP2	
G	OP1	

Note: A logic "1" on the anode drive signal line will activate the corresponding anode on LED and/or segment.

Table 8.5.1 : Anode Driver Signals

LED Display

The five LEDs are activated in the same way as the digits of the display, and the five lines OP1 to OP7 are used to activate their anodes. Table 8.5.1 indicates signal line allocation. The five LEDs have a common cathode driven from one of the D.K.D.

outputs (Q9).   A value of 9 within the D.K.D. counter allows
current to pass through to all the cathodes of the LEDs.

The clocking rate requirement for the D.K.D. (at least every 7.5
msecs) also applies for the LEDs.   Failure to meet this
requirement causes the LEDs to turn off due to the fact that the
counter will be automatically set to 15.

As can be seen by the above details, the signal lines OP1 to OP7
control the display of either one digit, or, any or all of the LEDs
at any one time.   The display and LEDs therefore require regular
refreshing to provide an apparent static display to the viewer.

Scanning the Switches

The 23 Keypad switches are arranged as a matrix for ease of
monitoring.   The matrix has 8 columns and 4 rows.   The columns
are activated by the D.K.D. via its counter.   The signals from the
D.K.D. connecting to the cathodes of digits 0 to 7 of the display
are also used to drive the columns.   The rows are read via signal
lines IP0 to IP4.   A particular keypad switch is read by activating
the column containing that switch, and by reading the appropriate
row from IP0 to IP3 to see if it is activated.   A logic zero read
from a row implies that the corresponding Key on the activated
column has been pressed.   For example, to sense if the key "6"
at the intersection of column Q3 (which also connects to digit 3)
and row 0 (which corresponds to signal line IP0) is being pressed,
the following is done.   The counter of the D.K.D. is clocked to a
count of 3.   The signal line IP0 is then read to see if it is at logic
"0".   If it is, then the key "6" is being pressed.

It should be noted that the output signals from the counter within
the D.K.D. used to drive the keyboard matrix columns are also
used to drive the cathodes of the digit display and LEDs with the
specified refresh requirement.

The two-position switch on the KDU is not on the matrix connecting the Keypad switches. The position of this switch is monitored by simply reading signal line IP4. This line is TTL compatible.

Table 8.5.2 gives the correlation between the KDU switches, the required values in the D.K.D. counter, and the pin numbers on the device connector carrying the sensing signals (IP0 to IP3).

Note: Only one key should be pressed at any one time.

8.5.4.2   Software Driver

The Utility program UPK provides all the necessary functions for using the PDM-KDU module, including the use of the DCE-PRG EPROM programmer modules. It provides sophisticated facilities for developing programs in machine language at minimum cost, and for program modification in the field. These functions include system initialization, display/modify memory locations and CPU registers, move and fill memory blocks, set-up or change the RAM vector addresses of interrupt service routines, initiate program execution, single-step and trace program execution by displaying all CPU registers after each instruction execution, and program EPROMs including compare-with-memory and transfer-to-memory functions.

The PDM-KDU can also be used as an I/O device for the input and output of hexadecimal data by using a suitable software driver routine. Section 8.5.6 gives an example of a complete software routine that enables the usage of the PDM-KDU as a normal input and output device.

KDU Switch	Count in D.K.D.	Device connector pin for sense signal (IP0 to IP3)
0	0	1
1	1	2
2	0	2
3	6	4
4	5	1
5	4	1
6	3	1
7	0	4
8	0	1
9	6	1
A	7	1
B	1	4
C	5	3
D	1	1
E	2	3
F	7	3
FCT	2	4
GO	5	4
REST	4	4
↓	7	4
STEP	0	3
MODE	1	3
↑	6	3
RUN/ RST	-	5
		RST: Sense '0' RUN: Sense '1'
Q0 of D.K.D.	0	7

Table 8.5.2 : Correlation between Switches, Counter Values and Sensing Signals.

8.5.4.3   Module Connector Definitions

The PDM-KDU includes a connecting cable with a 25-pin D-type female connector. It can be plugged directly into the device connector of any 8080 CPU based DCE microcomputer and can interface directly to the TICC parallel ports.

The pin definition of the 25-pin D-type female connector:

Pin Number	Signal
1	IP0
2	IP1
3	IP2
4	IP3
5	IP4
7	IP6
23	OP0
24	OP1
25	OP2
13	OP3
12	OP4
11	OP5
10	OP6
9	OP7
15	+5V
19	0V

Table 8.5.3 : PDM-KDU Connector Pin Definition

8. 5. 4. 4   <u>Operational Requirements</u>

<u>Power Requirements</u>

The PDM-KDU requires a single +5V power supply. When used with 8080 CPU based DCE microcomputers, this can be obtained directly from its device connector.

Maximum power requirement is:

+5V   :   200 mA

<u>Environmental Requirements</u>

Operating temperature $\leq$ 0°C to 55°C
Storage temperature   : -25°C to +85°C
Relative humidity   : upto 95 % non-condensing.

8. 5. 5.   <u>ORDERING INFORMATION</u>

PDM-KDU   : Standard version including connecting cable.

UPK   : The PDM-KDU oriented Utility program must be ordered separately (specify for which DCE microcomputer).

8.5.6   SOFTWARE DRIVER FOR PDM-KDU

```
;KDU INPUT/OUTPUT ROUTINE.
;D. A. I.
;

;THIS ROUTINE ALLOWS THE PROGRAMMER TO DISPLAY
;A SIMPLE TEXT ON THE KDU.
;IT ALSO PROVIDES A DATA ENTRY FACILITY.

;ONCE THE TEXT HAS BEEN TRANSFERED TO THE
;DISPLAY BUFFER, ITS OUTPUT IS CONTINUOUS & AUTOMATIC
;UNTIL THE INPUT ROUTINE IS TERMINATED BY THE OPERATOR
;OR BY THE TIME-OUT OPTION.

;OUTPUT.
;ON ENTRY, THE HL REGISTER PAIR IS SET TO POINT TO
;THE LOCATION OF THE TEXT TO BE DISPLAYED. IT IS
;IMPORTANT TO NOTE THAT THIS TEXT MUST BE STORED
;IN DISPLAY CODE (SEE TABLE "DIST" FOR EXAMPLES).

;INPUT.
;THE B REGISTER IS SET TO THE NUMBER OF DIGITS
;TO BE ENTERED (FIELD WIDTH), AND THE C REGISTER
;IS SET TO THE LEAST SIGNIFICANT DIGIT POSITION
;OF THE FIELD IN THE 9-DIGIT DISPLAY (POSITION
;0 IS AT THE LEFT, 8 AT THE RIGHT).

;DIGITS ENTERED ON THE KEYBOARD ARE SHIFTED LEFT
;THROUGH THE FIELD IN THE DISPLAY, AND THE HEX
;VALUE OF EACH DIGIT IS COPIED INTO A DATA BUFFER.

;THE ONLY KEYS VALID IN THIS ROUTINE ARE THE HEX DIGITS
;(0-9, A-F) AND THE "ROLL-UP" (^) KEY (TO END THE ENTRY).
;A NULL ENTRY (NULLE) FLAG IS SET IF THE ROUTINE IS
;TERMINATED BY THE ROLL-UP KEY BEFORE ANY DIGITS
;HAVE BEEN ENTERED.
```

```
;EXAMPLE: -

;LXI     H, CHMSG                        ;DISPLAY "CH-          ".
;THIS ASKS FOR A CHANNEL NUMBER.
;MVI     B, 2                 ;2 DIGITS IN FIELD.
;MVI     C, 4                 ;ENTRY POINT IN DISPLAY,
;I. E.  5TH POSITION FROM LEFT.
;CALL    KDUIO                ;CALL ROUTINE.
;MOV     A, M                 ;RETRIEVE MS DIGIT.
;INX     H                    ;POINT TO NEXT LS DIGIT.
;ADD     A
;ADD     A
;ADD     A
;ADD     A                    ;MULTIPLY BY 16.
;ADD     B                    ;ADD LS DIGIT.
;STA     CHANNEL                         ;SAVE BINARY VALUE OF CHANNEL.

;THE "KDU BUFFER AREA" ORIGIN CAN BE MOVED TO
;SUIT YOUR PROGRAM.

;SUBROUTINES : -

;DISP    DISPLAY DRIVER, KEYBOARD SCAN & DECODE.
;XFER    MOVE TEXT (H, L) TO DISPLAY BUFFER.
;DISPA   SETS UP TIMER INTERRUPT THEN JUMPS TO DISP.
;DISPI   INTERRUPT ROUTINE.
;TRAD    TRANSLATE HEX BYTE TO 2 DISPLAY CHARACTERS.
;TRSP    TRANSLATE HEX DIGIT TO DISPLAY CHARACTER.
```

```
;APART FROM ITS USE IN "KDUIO", THE "DISP"
;SUBROUTINE CAN BE USED ON ITS OWN (TO ALLOW ENTRY OF
;SINGLE DIGITS WITH NO COPY TO THE DISPLAY), OR
;WITH THE TIME-OUT TO END THE WAIT-FOR-KEY LOOP
;IN "DISP".  IN THIS CASE, THE PROGRAM FOLLOWING
;THE CALL ON "DISPA" WOULD CHECK THE ZERO FLAG.
;IF IT IS SET, THEN A TIME-OUT HAD OCCURED.  OTHERWISE
;THE "A" REGISTER CONTAINS THE HEX DIGIT ENTERED
;(0-9, A-F).

;EXAMPLE.
;THE PROGRAM READS A CHANNEL OF AN ANALOG INPUT CARD
;AT 100 MS INTERVALS.  A NEW CHANNEL CAN BE SELECTED
;WITH THE KDU.  NOTE THAT "COUNT" IS RELOADED BEFORE
;EVERY CALL OF DISPA.  THIS ALLOWS VARIOUS
;TIME INTERVALS TO BE SET UP AT DIFFERENT POINTS
;IN THE PROGRAM.


;LOOP:    MVI      A, 10            ;10*10 MS
;         STA      COUNT           ;SET TIME-OUT COUNTER.
;         CALL     DISPA           ;(MIN TIME = 10 MS).
;         JNZ      NEW             ;KEY PRESSED.  SET NEW CH.
;         CALL     READ            ;READ ANALOG CARD.
;         JMP      LOOP
;NEW:     STA      CHAN            ;SET UP NEW CHANNEL.
;         JMP      LOOP
```

```
;KDUIO.

KDUIO:  PUSH    B               ;SAVE DIGITS, POSITION.
        CALL    XFER            ;MOVE TEXT TO DISPLAY.
        MVI     A,1
        STA     NULLE           ;PRESET NULL ENTRY FLAG.
        MVI     B,10            ;CLEAR DATA BUFFER.
        LXI     H,DATAB
KDIOG:  MVI     M,0
        INX     H               ;STEP POINTER.
        DCR     B               ;COUNT DOWN
        JNZ     KDIOG           ;LOOP FOR MORE.

KDIOF:  POP     B               ;RETRIEVE DIGITS, POSITION.
KDIOB:  CALL    DISP            ;DISPLAY MESSAGE, WAIT FOR KEY.
        CPI     ROLU            ;CHECK IF ^.
        JZ      KDIOH           ;RETURN IF SO.
        MOV     D,A             ;SAVE DIGIT.
        ANI     OFOH            ;TEST FOR CONTROL DIGIT.
        JNZ     KDIOB           ;IGNORE IF SO.

        STA     NULLE           ;CLEAR NULL ENTRY FLAG.
        MOV     A,D             ;RETRIEVE DIGIT.
        PUSH    PSW             ;SAVE ON STACK.

        LXI     H,DISB          ;PUT DIGIT IN DISPLAY BUFFER.
        MVI     D,0             ;ADD DIGIT ENTRY POSITION.
        MOV     E,C             ;TO BUFFER BASE.
        DAD     D
        MOV     D,M             ;SAVE OLD DIGIT.
        PUSH    D

        CALL    TRSP            ;TRANSLATE & STORE DIGIT.
        POP     D               ;RETRIEVE OLD DIGIT.
        DCX     H               ;TO OFFSET INX H IN TRSP.
        PUSH    B               ;SAVE DIGITS, POSITION.
```

```
KDIOC:    DCX      H                    ;NEXT MS BUFFER POSITION.
          DCR      B                    ;COUNT DOWN "DIGITS".
          JZ       KDIOD                ;IF END OF SHIFT.
          MOV      E, M                 ;SAVE OLD DIGIT.
          MOV      M, D                 ;REPLACE WITH NEW DIGIT.
          MOV      D, E                 ;SET FOR NEXT SHIFT.
          JMP      KDIOC


KDIOD:    POP      B                    ;RETRIEVE "DIGITS", "POSITION".
          POP      PSW                  ;AND LATEST DIGIT.
          LXI      H, DATAB                    ;POINT TO DATA BUFFER.
          MVI      D, 0                 ;ADD "POSITION".
          MOV      E, C
          DAD      D
          MOV      D, M                 ;SAVE OLD DIGIT.
          MOV      M, A                 ;REPLACE WITH NEW ONE.
          PUSH     B                    ;SAVE B, C.

KDIOE:    DCX      H                    ;POINT TO NEXT MS POSITION.
          DCR      B                    ;COUNT DOWN "DIGITS".
          JZ       KDIOF                ;END OF SHIFT.
          MOV      E, M                 ;SAVE OLD DIGIT.
          MOV      M, D                 ;REPLACE WITH NEW ONE.
          MOV      D, E                 ;SAVE OLD ONE FOR NEXT SHIFT.
          JMP      KDIOE                ;LOOP FOR MORE.

KDIOH:    LXI      H, DATAB                    ;POINT TO DATA BUFFER.
          MOV      A, C                 ;ADD "POSITION".
          SUB      B                    ;SUB "DIGITS"-1.
          INR      A
          MOV      E, A
          MVI      D, 0                 ;MOVE TO D, E.
          DAD      D
          RET                           ;RETURN.
                                        ;H, L POINTS TO MS DATA DIGIT.
```

```
; XFER.  MOVE TEXT TO DISPLAY.

XFER:     LXI     D, DISB              ; POINT TO BUFFER.
          MVI     B, 10               ; SET TO MOVE 10 CHARS.
XFERA:    MOV     A, M                ; GET TEXT CHAR.
          STAX    D                   ; MOVE TO DISPLAY.
          INX     H
          INX     D                   ; STEP POINTERS.
          DCR     B                   ; COUNT DOWN.
          JNZ     XFERA               ; MORE.
          RET


          ; DISPA.
          ; SET TICC FOR TIMER 3 INTERRUPTS.
          ; SET TIME-OUT, AND JUMP TO "DISP".

          ; PUT "JMP DISPI" AT ORIGIN 18H

DISPA:    XRA     A
          STTCM
          MVI     A, 9
          STTCM                       ; SET TICC FOR INTS.
          MVI     A, 8
          STIMR                       ; ALLOW TIMER 3 INT.
          MVI     A, OAOH             ; SET TIMER 3 FOR 10 MS.
          STTIM   3
          EI
          JMP     DISP                ; GO TO DISPLAY ROUTINE.

DISPI:    PUSH    PSW                 ; TIMER 3 INT. ROUTINE.
          MVI     A, OAOH
          STTIM   3                   ; RELOAD TIMER 3.
          LDA     COUNT
          DCR     A
          STA     COUNT               ; COUNT DOWN "VALUE".
          JZ      TMOUT               ; TIME-OUT.
          POP     PSW
          EI
          RET                         ; NORMAL RETURN.
TMOUT:    POP     PSW                 ; STRAIGHTEN STACK.
          POP     PSW                 ; DISCARD INT. RETURN ADDR.
          XRA     A                   ; CLEAR A-REG.
          RET                         ; TO CALL OF "DISP".
```

```
                ;DISP STEPS THE DISPLAY AND CHECKS FOR KEYBOARD INPUT.

DISP:   LHLD    DISBP           ;DISPLAY BUFFER POINTER
        MVI     A,0             ;TO CLOCK KDU
        STOUT                   ;OUTPUT TO KDU
        LDIN                    ;TO CHECK ROW ONE
        ANI     040H            ;SEE IF ROW ONE
        JNZ     DROW1           ;IF SO RELOAD POINTER
        LXI     H,DISB          ;WITH BUFFER START
DROW1:
        MOV     A,M             ;COLLECT DISPLAY DATA
        ORI     061H            ;SET CLOCK BIT
        STOUT                   ;SEND TO KDU
        INX     H               ;INDEX TO NEXT DISPLAY
        SHLD    DISBP           ;PUT IN STORE
        LXI     D,KEYB-DISB-1   ;INCREMENT TO KEY INPUT
        DAD     D               ;FOR INPUT COMPARE
        LDIN                    ;READ KEY INPUT
        ANI     00FH            ;ISOLATE BITS
        XRI     00FH            ;AND COMPLEMENT
        CMP     M               ;COMPARE WITH LAST RESULT
        MOV     M,A             ;AND UPDATE STORED RESULT

        JZ      DISP            ;JUMP IF NO CHANGE
        LXI     D,-KEYB                 ;TO SUBTRACT BASE
        DAD     D               ;LEAVING INDEX
        DAD     H               ;MULTIPLY BY FOUR
        DAD     H
        ANI     0FH             ;REMOVE TOP BITS
        JZ      DISP            ;JUMP IF NO INPUT
DROW2:
        INR     L               ;CYCLE TO COUNT WHICH BIT IS SET
        RAR
        JNC     DROW2
        MVI     H,0             ;COMPLETE INDEX
        LXI     D,KC-1          ;KEYBOARD TABLE
        DAD     D               ;ADD INDEX
        MOV     A,M             ;FINAL CODE
        RAL                     ;CHECK CONTROL BIT
        MOV     A,M             ;FINAL CHARACTER AGAIN
        RNC                     ;EXIT IF NO CARRY
        ANI     07FH            ;CLEAR TOP BIT
        JZ      DISP            ;NO INPUT - LOOP
        MOV     A,M             ;FINAL CHARACTER
        RET
```

```
;          DISPLAY CODES

;          DIGIT     HEX. CODE     SEGMENTS
;
DIST:
DSC0     EQU     OFCH              ; ABCDEF
         DB      DSC0
DSC1     EQU     060H              ;  BC
         DB      DSC1
DSC2     EQU     ODAH              ; AB DE G
         DB      DSC2
DSC3     EQU     OF2H              ; ABCD  G
         DB      DSC3
DSC4     EQU     066H              ;  BC  FG
         DB      DSC4
DSC5     EQU     OB6H              ; A CD FG
         DB      DSC5
DSC6     EQU     OBEH              ; A CDEFG
         DB      DSC6
DSC7     EQU     OEOH              ; ABC
         DB      DSC7
DSC8     EQU     OFEH              ; ABCDEFG
         DB      DSC8
DSC9     EQU     OE6H              ; ABCD FG
         DB      DSC9
DSCA     EQU     OEEH              ; ABC EFG
         DB      DSCA
DSCB     EQU     O3EH              ;   CDEFG
         DB      DSCB
DSCC     EQU     O9CH              ; A  DEF
         DB      DSCC
DSCD     EQU     O7AH              ;  BCDE G
         DB      DSCD
DSCE     EQU     O9EH              ; A  DEFG
         DB      DSCE
DSCF     EQU     O8EH              ; A   EFG
         DB      DSCF
DSCH     EQU     O6EH              ;   C EFG
DSCI     EQU     O20H              ;    D
DSCO     EQU     O3AH              ;    CDE G
DSCS     EQU     OB6H              ; A CD FG
DSCP     EQU     OCEH              ; AB  EFG
DSCR     EQU     OOAH              ;     E G
DSCU     EQU     O7CH              ;  BCDEF
DSCL     EQU     O1CH              ;     DEF
ROLU     EQU     O10H
```

```
;       KEYBOARD CODES
                                  ; SELECT        RETURN
KC:     DB      08H               ; O             1
        DB      02H               ; O             2
        DB      CSTEP             ; O             4
        DB      07H               ; O             8
        DB      ODH               ; 1             1
        DB      01H               ; 1             2
        DB      CMODE             ; 1             4
        DB      OBH               ; 1             8
        DB      OOH               ; 2             1
        DB      080H              ; 2             2
        DB      OEH               ; 2             4
        DB      CFUN              ; 2             8
        DB      06H               ; 3             1
        DB      080H              ; 3             2
        DB      080H              ; 3             4
        DB      080H              ; 3             8
        DB      05H               ; 4             1
        DB      080H              ; 4             2
        DB      080H              ; 4             4
        DB      CREST             ; 4             8
        DB      04H               ; 5             1
        DB      080H              ; 5             2
        DB      OCH               ; 5             4
        DB      CGO               ; 5             8
        DB      09H               ; 6             1
        DB      080H              ; 6             2
        DB      ROLU              ; 6             4
        DB      03H               ; 6             8
        DB      OAH               ; 7             1
        DB      080H.             ; 7             2
        DB      OFH               ; 7             4
        DB      ROLD              ; 7             8
        DB      080H              ; 8             1
        DB      080H              ; 8             2
        DB      080H              ; 8             4
        DB      080H              ; 8             8
;
CSTEP   EQU     088H
CMODE   EQU     086H
CFUN    EQU     082H
CREST   EQU     040H
ROLU    EQU     010H
ROLD    EQU     020H
CGO     EQU     084H

;       END KEYBOARD CODES
```

```
                    ; TRSP.  TRANSLATE & STORE ONE DISPLAY CHARACTER.

TRSP:    ANI     OFH             ; LS4 ONLY
         LXI     D, DIST         ; TRANSLATE TABLE.
         ADD     E
         MOV     E, A            ; SET INDEX.
         JNC     TRNC
         INR     D
TRNC:    LDAX    D               ; GET TRANSLATION.
         MOV     M, A            ; PUT INTO BUFFER.
         INX     H
         XRA     A               ; CLEAR A-REG.
         RET

; KDU BUFFER AREA
;
         ORG     1000H

DISB:    DS      16              ; DISPLAY BUFFER
KEYB:    DS      16              ; KEY BUFFER.
DISBP:   DS      2               ; BUFFER POINTER
DATAB:   DS      9               ; DATA BUFFER
COUNT:   DB      0               ; COUNTER
NULLE:   DB      0               ; NULL ENTRY FLAG.
;
         END
```

Note on KEYBOARD CODES Table in Page 8-36:

The entry 080H in this table indicates an unused position within
the keyboard matrix.   The Function keys are indicated by
'CSTEP', 'CMODE' etc. , and they are equated to their actual
values.   These Function codes correspond to the actual Function
keys of the PDM-KDU as follows:

CSTEP	=	STEP
CMODE	=	MODE
CFUN	=	FCT
CREST	=	REST
ROLU	=	Upward arrow
ROLD	=	Downward arrow
CGO	=	GO

The RUN - RST switch is not used in this example.

8. 6   PDM-KBD : HEAVY-DUTY KEYBOARD

8. 6. 1   FUNCTIONAL DESCRIPTION

The PDM-KBD heavy-duty keyboard module provides 24
momentary-contact type keys, arranged in a 6 x 4 matrix.
Each key has a diode in series with it for column isolation
during scanning. All the columns can be activated together
to determine if any keys have been pressed, before scanning
to identify them individually.

The module can be driven directly from the parallel input
and output ports available at the device connector of all
8080 CPU based DCE microcomputers. It can also be
driven via the RWC interface modules with parallel interfaces.

Two of the signal lines together with +5V and ground are
available at a 4-pin male connector, which enables an
external device such as the PDM-DSP display module to be
directly connected to the PDM-KBD.

An optional kit enables the keyboard module to be directly
mounted at the front or back of any DAI eurobox or eurorack.

8. 6. 2   FEATURES

° 24 keys arranged in a 6 x 4 matrix.

° Series diode with each key for column isolation during scanning.

° Parallel interface connection to DCE microcomputer, or
  suitable Real-World module.

° 4-pin connector for driving the PDM-DSP display module, or
  similar device.

° Removable transparent key tops, for user definition of key
  symbols.

° Keys assembled on a 100 x 160 mm metal mounting plate.

° Optional kit for direct mounting on any DAI eurobox or
  eurorack.

8.6.3 FUNCTIONAL BLOCK DIAGRAM
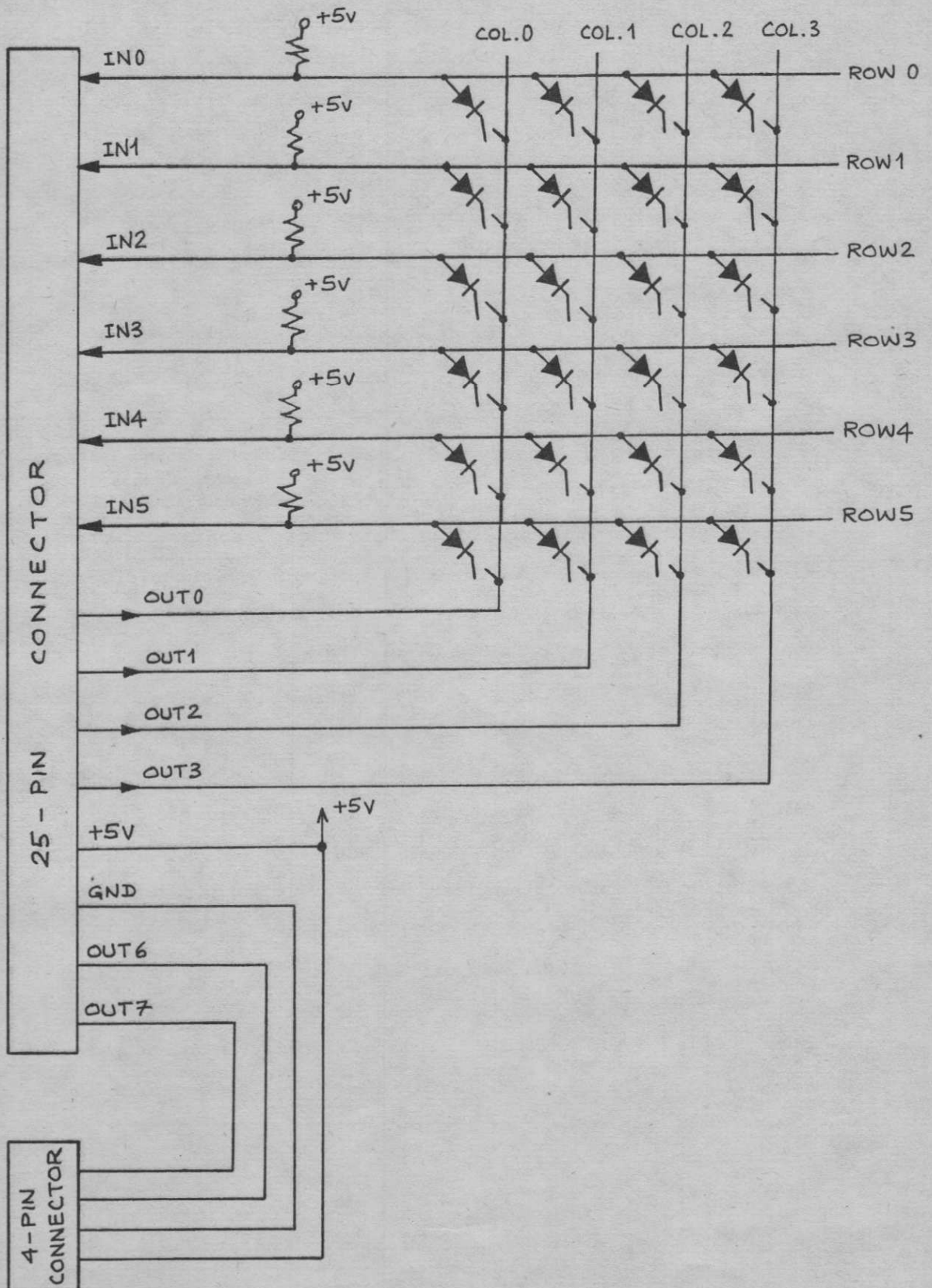
8.6.4   SYSTEM DESIGN PARAMETERS

8.6.4.1   Hardware Configuration

Section 8.6.3 shows a functional block diagram of the Heavy-
duty Keyboard module. The module contains 24 momentary-
contact type keys arranged in a 6 x 4 matrix. Each key has
a diode in series with it for column isolation during scanning.
All the keyboard matrix columns can be activated together
if sufficient current can be sunk by the column drivers. This
can be used to check if any key has been pressed, before
scanning the keyboard. If a key has been pressed, the
keyboard can be scanned column by column to identify that key.

The 4 columns of the keyboard matrix must be driven via the
signal lines OUT0 to OUT3. The closing of a key is monitored
by driving its column with a logic 0. If upon reading its row
a logic 0 is detected, the key at the junction of the selected row
and column has been pressed. The 6 rows of the keyboard
matrix are read via the signal lines IN0 to IN5. The loading
on each of these input lines is one TTL load.

The 4 column driver signal lines and the 6 row scanning signal
lines are brought to a 25-pin D-type female connector on the
module. It also has a 4-pin male connector which enables an
external device to be physically linked to it. These 4 lines
are directly routed to the 25-pin connector, and two of them
are used for +5V supply and ground.

The PDM-KBD module can be driven directly from the parallel
TICC input and output ports available at the device connectors
of 8080 CPU based DCE microcomputers.

In this case, two of the output lines together with +5V and ground will be available at the 4-pin connector. The large 9-digit display module PDM-DSP can be directly connected to this 4-pin connector, in which case the two output signal lines OUT6 and OUT7 must carry a clock signal and serial data to it. The keyboard module and any external device connected via the 4-pin connector can also be driven via any suitable Real-World interface module.

Figure 8. 6. 1 gives the dimensions of the metal supporting plate for the 24 keys. An optional packaging kit PSM-KBD/M enables the keyboard module to be directly mounted at the front or back of any DAI eurobox or eurorack, with four quarter-turn screws. It mounts the keyboard horizontally (4 rows of 6 keys) using a 203 mm wide panel. The keys have removable transparent keytops to enable user definition of key symbols.

8. 6. 4. 2   Module Connector Definitions

The PDM-KBD module includes a 25-pin D-type female connector. This may be connected directly to the device connector of any 8080 CPU based DCE microcomputer. Table 8. 6. 1 shows the connector pin definitions, together with the corresponding TICC signals when connected to a DCE microcomputer. This table also gives the pin definitions for the 4-pin male connector on the module. It is situated next to the 25-pin connector, and its pin adjacent to the 25-pin connector is designated pin 4.

Signal Name	Description	TICC Signal	Pin Number
IN0	Matrix Row 0	TICC Input Port Bit 0	1
IN1	1	Bit 1	2
IN2	2	Bit 2	3
IN3	3	Bit 3	4
IN4	4	Bit 4	5
IN5	5	Bit 5	6
OUT0	Matrix Column 0	TICC Output Port Bit 0	23
OUT1	1	Bit 1	24
OUT2	2	Bit 2	25
OUT3	3	Bit 3	13
OUT6	To 4-pin connector pin 1	Bit 6	10
OUT7	To 4-pin connector pin 3	Bit 7	9
+5V	+5V to PDM-KBD and to 4-pin connector pin 4		15
GND	To 4-pin connector pin 2		19

Note: The TICC Signals are applicable only when the PDM-KBD is directly connected to a suitable DCE microcomputer.

Table 8. 6. 1 : PDM-KBD Connector Pin Definitions

8. 6. 4. 3   Operational Requirements

Power Requirements

The PDM-KBD requires a single +5V power supply. When used with 8080 CPU based DCE microcomputers, this can be obtained directly from its device connector.

When the columns on the key matrix are not driven to logic 0, the power supply requirements are negligible. When a column is driven to logic 0, for each key closed on that column, the power supply requirement is approximately 4. 2 mA.

Column Driver Signal Requirements

The 4 columns in the key matrix must be driven via signals OUT0 to OUT3. If an output line is driven to logic 0, for each key closed on the column the buffer driving the output line must sink 5. 6 mA. If an output line is driven to logic 1, the current to be supplied by the driving buffer is negligible.

Environmental Requirements

Operating Temperature	: 0°C to 55°C
Storage Temperature	: -25°C to +85°C
Relative Humidity	: upto 95 % non-condensing

8. 6. 5   ORDERING INFORMATION

PDM-KBD	: Standard version.
PSM-DCC/25	: The optional connecting cable to a DCE microcomputer must be ordered separately.

PSM-FCC/4   : The optional connecting cable for the
                       4-pin connector must be ordered
                       separately. It is 40 cm long, and has
                       two female connectors at the ends.

PSM-KBD/M   : The optional packaging kit for mounting
                       the keyboard on any DAI eurorack or
                       eurobox must be ordered separately.

8.7 PDM-DSP : LARGE DIGIT DISPLAY

8.7.1 FUNCTIONAL DESCRIPTION

The PDM-DSP display module provides nine large 7-segment LED displays with decimal points, and eight LED indicators. The LED digits are each 7,62 mm high and 4,78 mm wide. They can be used to display hexadecimal data, and a limited character set. The eight LED indicators are mounted in a line, and can be used to identify different modes of operation etc. The entire module is covered by a thick red filter mounted in front, for protection and enhanced display legibility.

The module must be driven serially by data and clock signals, supplied via the 4-pin male connector. The remaining two pins are for a +5V supply and ground. The clock signal is used to transfer the serial data to an 80-bit shift-register on the module. The seven segments and the decimal point of each of the nine digits, and the eight indicators are driven in accordance with the data bits stored in this shift register. Once the shift-register is loaded with the necessary bit pattern, the corresponding display will remain stable until new data is clocked into the shift-register by driver software.

The display module can be directly connected to the PDM-KBD keyboard, or to any other suitable interface, via a separate 4-wire flat-cable connection. An optional kit enables the display module to be directly mounted at the front or back of any DAI eurobox or eurorack, with four quarter-turn screws. The width of the mounting panel is 137 mm, which is exactly one-third that of a 19-inch rack or box.

8.7.2   <u>FEATURES</u>

    ° 9 large 7-segment LED displays with decimal points.

    ° 8 LED indicators.

    ° 4-pin connector for serial interface and power.

    ° Static operation with no data refresh requirements.

    ° Directly connectable to the PDM-KBD keyboard module.

    ° Red cover filter for enhanced legibility and protection.

    ° Optional kit for direct mounting on any DAI eurobox or
       eurorack.

8. 7. 3   FUNCTIONAL BLOCK DIAGRAM
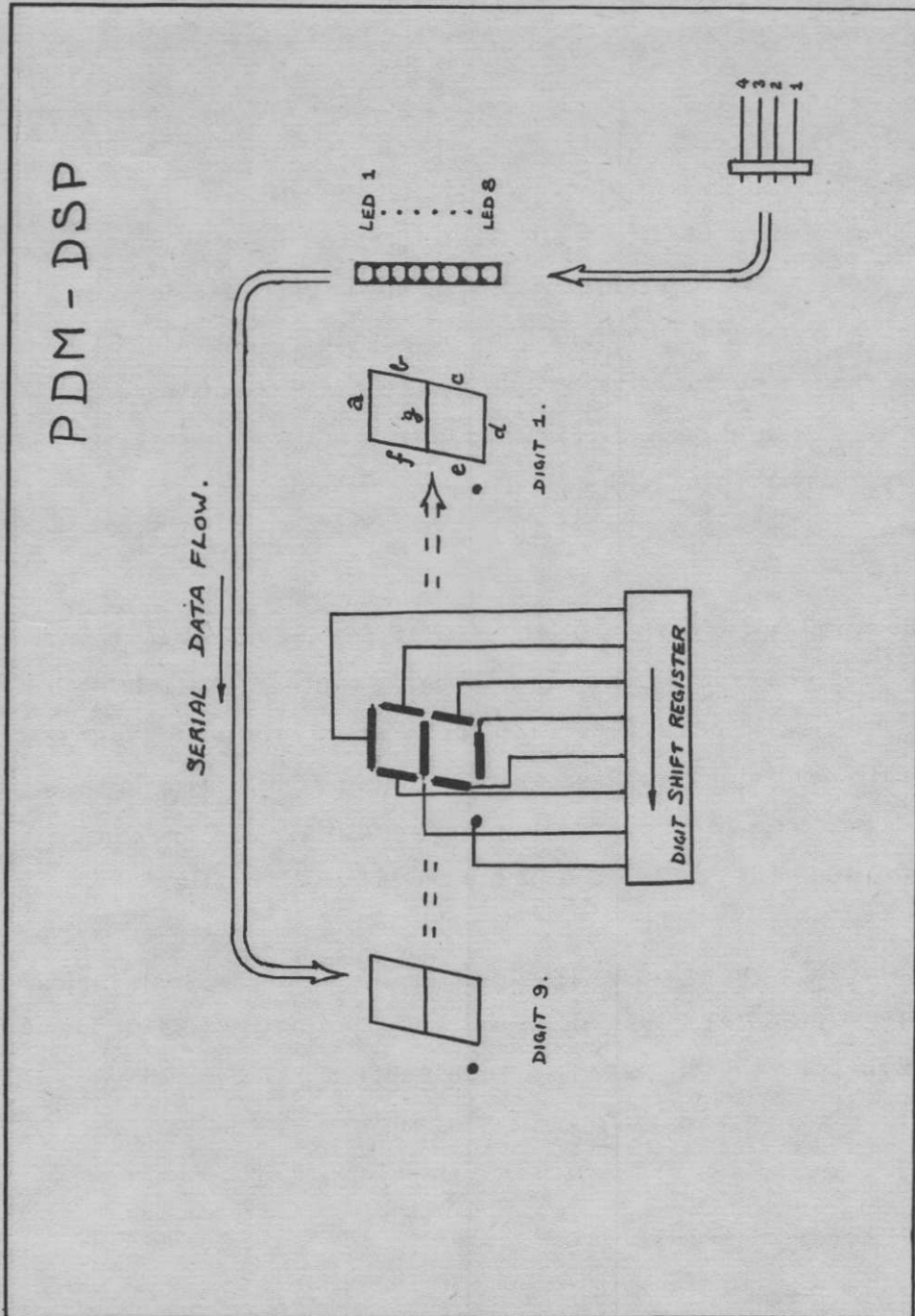
8.7.4   SYSTEM DESIGN PARAMETERS

8.7.4.1   Hardware configuration

The functional block diagram in section 8.7.3 illustrates the hardware configuration.

Each individual segment, decimal-point, or indicator LED is driven by an output of the 80 bit, static, shift register memory. Thus, synchronous communications in bit-serial form can be acheived with only two latched TTL output lines from the DCE system. These outputs are driven by the system software to operate as data and data-clock lines to this shift register. Typically, two of the TICC output lines are dedicated for this purpose.

Since the displays are controlled in a bit-per-segment fashion, non-numeric characters can also be represented. This includes most alphabetical characters, and therefore system messages can usually be displayed. Since all the decimal digits, and the letters A to F can be represented; hexadecimal data presentation is thus an inherent application of the PDM-DSP module.

Data is shifted at every 0 to 1 transition of the data-clock input. Data is first transferred through the eight indicator LED's, and then through the digits 9 to 1 (see section 8.7.3). The individual segment sequence is given below:

1st bit shifted in display decimal point or indicator N° 3

2nd bit shifted in display segment g   or indicator N° 4

3rd	"	"	f	"	N° 6
4th	"	I'	e	"	N° 5
5th	"	"	d	"	N° 8
6th	"	"	c	"	N° 1
7th	"	"	b	"	N° 2
8th	"	"	a	"	N° 7

Note: 1) The LED indicators are not loaded in sequence.

2) As each bit is shifted in, ALL 80 segments take the old status of their predecessors.

Table 1. : Bit/segment relationship

An all cases, a logic zero is needed to illuminate the selected segment.

Selection of required digit

Since data must pass through all previous stages in the shift register, before it arrives at its required destination, extra clock pulses must be given. These are generally those used to shift the remaining data into the module.   However, for reference the following table of counts has been prepared.

Digit position required for bit-pattern	Number of clock pulses required after 8-bit data has been shifted in.
9	8
8	16
7	24
6	32
5	40
4	48
3	56
2	64
1	72
Indicator LED's	0

Table 2: Post-clock counts for display positions

8.7.4.2   Connector Details

Connector pin configuration

pin 1   clock, transfers data on low to high transition.

pin 2   ground

pin 3   serial data, 0 to illuminate the required segment.

pin 4   +5V supply.

A 4 wire flat cable with suitable connectors is available. This cable, type N° PSM-FCC/4, is suitable to connect the PDM-DSP module to the connector provided on the PDM-KBD module.

8. 7. 4. 3   Operational Requirements

Signal characteristics

The signal levels conform to standard TTL logic levels.
The inputs impose the following loading on their respective
drivers:

Clock input: Logic 0, sink 14. 4mA max.
                    Logic 1, source 360 µA max.

Data input: Logic 0, sink 3. 2 mA max.
                    Logic 1, source 80 µA max.

Signal timing

Data bits can be shifted into the PDM-DSP module at upto
25 MHZ.   Thus, maximum DCE system speed can be
accomodated.
However, the data must be written at least 15 nS before the
rising edge of the clock.   Thus, the data bit should be written
with the clock output set low, and then a second instruction
should transfer the clock level from 0 to 1.

Power requirements

The PDM-DSP module typically consumes 60 mA from the
single +5V supply.

Environmental Requirements:

Operating temperature   : 0°C to 55°C
Storage temperature   : -25° to 85°C
Relative humidity   : 95 % non-condensing.

8.7.5   <u>ORDERING INFORMATION</u>

    PDM-DSP   : Standard version, with red filter plate.

    PSM-FCC/4   : The 4-wire flat-cable connection, must
                                 be ordered separately.

    PSM-DSP/M   : The optional packaging kit for mounting
                                 the display module on any DAI eurorack
                                 or eurobox must be ordered separately.