7.9 RWC-CCE : COMMUNICATIONS CONTROL ELEMENT

7.9.1 FUNCTIONAL DESCRIPTION

The RWC-CCE Real-World interface module allows the DCE processor to control 2 independent serial communication channels, software definable for synchronous or asynchronous communication with programmable Baud rates.

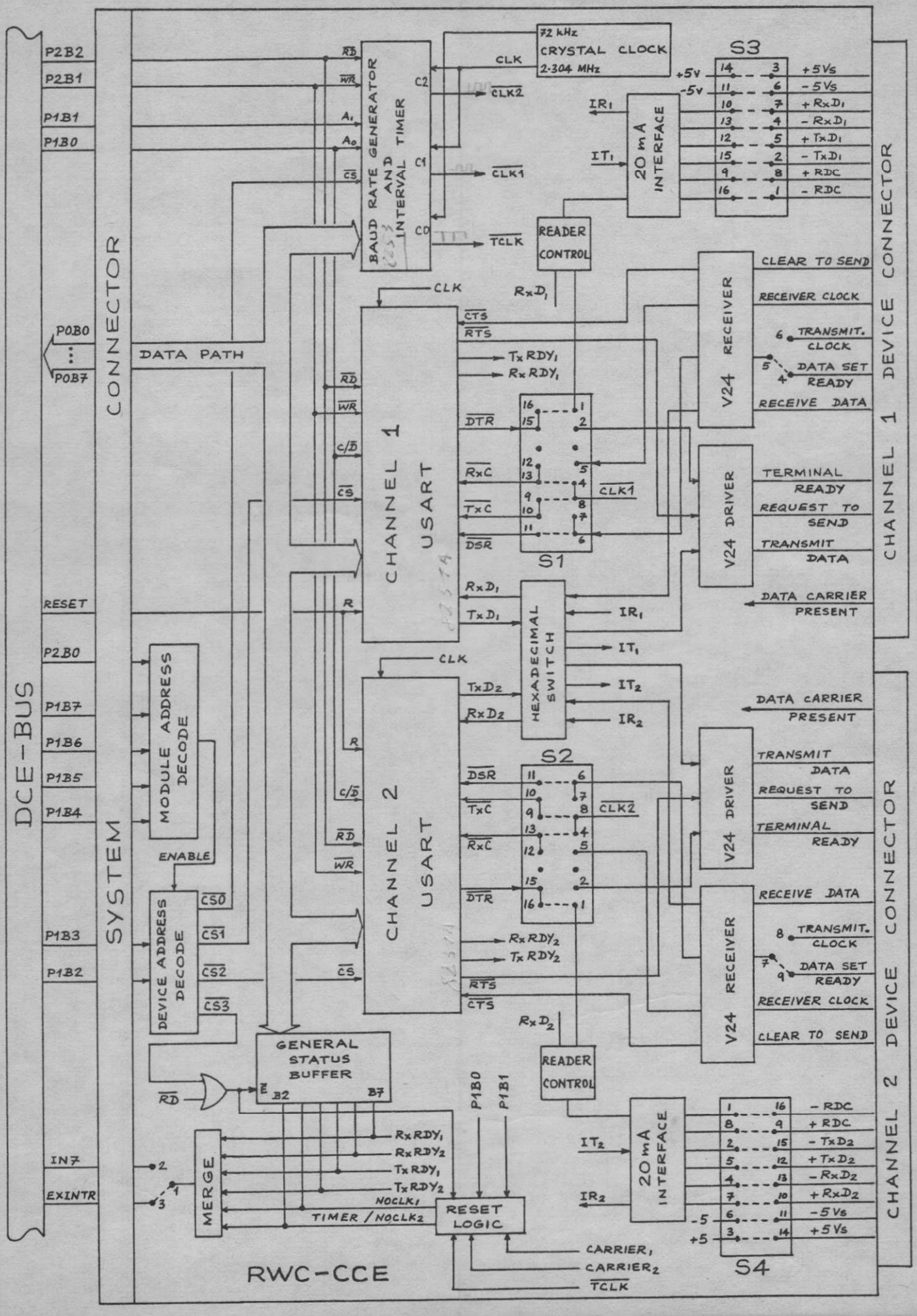
It provides two independent serial data communication channels between V24 or 20mA current data lines and the DCE-BUS. Each channel is independently software definable for synchronous or asynchronous protocols and Baud rates. Common protocol programs including IBM Bi-Sync are available. RWC-CCE can be used to communicate with large computers and for terminal cluster data concentration applications etc.

Each module has an identification address defined by a hexadecimal switch, and up to fifteen cards may be directly connected to the DCE-BUS.

7.9.2 FEATURES

- 2 independent serial communication channels.
- each channel independently software definable for synchronous or asynchronous communication.
- each channel independently programmable for different Baud rates.
- crystal controlled time-base.
- 2 separate standard V24 connectors.
- jumper selectable 20mA current loop or V24 interface.
- each channel with separate TTY reader relay control.
- one interval timer.
- interrupt register to merge 6 CCE interrupts into a single DCE interrupt request.
- uses standard DCE power supplies.

7.9.3 FUNCTIONAL BLOCK DIAGRAM



- standard hardware and software interface to DCE-BUS.
- selectable card address.
- single 100 x 160 mm eurocard format.

7.9.4 SYSTEM DESIGN PARAMETERS

7.9.4.1 Hardware Configuration

The functional block diagram in Section 7.9.3 illustrates the hardware configuration. The module does not use a single device RIC for interfacing to the DCE-BUS.

A programmable interval timer device (8253) is used to realize the two baud rate generators (counters 1 and 2 operating in Mode 3), as well as the interval timer (counter 0 operating in Mode 2). Counter 1 of this device produces a programmable clock signal which may be used as the Transmitter and Receiver Clocks for the Channel 1 USART. Counter 2 is used similarly with the Channel 2 USART. The Gate inputs to all three counters are tied to logic 1.

A crystal controlled clock circuit on the module produces a 72 kHz signal for the interval timer generation (counter C0), and a 2.304 MHz signal for the two baud rate generators (counters C1 and C2).

The two communication channels are implemented using two 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) devices. These USART devices can accept data characters from the DCE-BUS in parallel format and then convert them into a continuous serial data stream for transmission. Simultaneously they can receive serial data streams and convert them into parallel data characters for the DCE processor. They can be programmed to operate using virtually any serial data transmission technique presently in use, including IBM

Bi-Sync. They are capable of Synchronous and Asynchronous operation with software programmable Baud rates. The DCE processor can read the complete status of these USART devices at any time.

In addition to the status register within each USART, the RWC-CCE card has a General Status Buffer. The 6 input status signals to this buffer (one of which is the interval timer), can be made to generate a common interrupt request to the DCE processor. Following such an interrupt, DCE software can strobe the General Status Buffer and determine the interrupt source with a single Read operation. Polled operation is also possible where the DCE software periodically scans the content of this status buffer, for various status conditions including interval timer time-out.

The two serial communication channels may each be configured easily for 20mA current loop or V24 interface, via a hexadecimal switch and jumper link pads. Various signal options are provided for the V24 interface.

7.9.4.2 Programming Specifications

The RWC-CCE module is addressed via the standard DCE-BUS interface. Programming specifications for driving the DCE-BUS are given in Section 4.1.

The module does not have the usual single device RIC interface to the DCE-BUS. In addition to the 4-bit card address, it has a 2-bit device address which is decoded to select one out of the four logic sub-systems on the module. Another 2 bit address provides for register select within these devices. This 8-bit card/device address received from DCE GIC Port 1 via the DCE-BUS, is interpreted as follows:

b7 - b4 = card select address (1 to F)

b3 - b2 = device select address (0to3)

b1 - b0 = internal register select within the programmable Baud rate generator and interval timer (0 to 3).

b1 = reset interrupt due to modem clock failure on Channel 2, or interval timer time-out

b0 = Control/Data read write control for the two USART devices,
and
reset interrupt due to modem clock failure on Channel 1.

For module activation the card select address must correspond to the setting of the hexadecimal address switch located near the System Connector. When the module is correctly addressed the two device select address bits are decoded to enable one of the four logic sub-systems as follows:

P1B3	P1B2	ACTIVE SIGNAL	ACTIVE DEVICE
0	0	$\overline{CS0}$	Baud Rate Generator/Interval Timer
0	1	$\overline{CS1}$	USART for Channel 1
1	0	$\overline{CS2}$	USART for Channel 2
1	1	$\overline{CS3}$	General Status Buffer, when $\overline{RD}$ is active

Table 7.9.1 : Device Select Address Table for RWC-CCE

The enable signal for the General Status Buffer is used in conjunction with address bits b0 and b1 to reset two interrupt conditions, as shown in the functional block diagram in Section 7.9.3.

Baud Rate Generator and Interval Timer

This device has three counters C0, C1, C2, which may be software configured for different modes of operation. Counter C0 must be configured in Mode 2 to provide the interval timer signal. Counters C1 and C2 must be configured in Mode 3 to provide the Transmitter and Receiver clocks for the two USART devices. Table 7.9.2 gives the addressing for communications with Counters and Control Word Register on the device:

ADDRESS (HEX)	$\overline{RD}$	$\overline{WR}$	OPERATION
Y0	1	0	Load Counter C0
Y1	1	0	Load Counter C1
Y2	1	0	Load Counter C2
Y3	1	0	Write Mode Control Word
Y0	0	1	Read Counter C0
Y1	0	1	Read Counter C1
Y2	0	1	Read Counter C2
Y3	0	1	Illegal
Y0-Y3	1	1	No-Operation; 3-state
Y4-YF	X	X	Disable ; 3-state

Notes

1. Y is the card address select switch setting in hex (1 to F).
2. X means don't care.
3. RDRWC and WRRWC software routines provide the $\overline{RD}$ and $\overline{WR}$ signals accordingly.

Table 7.9.2 : Register Addresses for the Baud Rate Generator and Interval Timer

Each of the three counters C0, C1, C2 is individually configured by writing a Mode Control Word into the common control word register (address Y3). The Mode Control Words for the three counters are as follows:

34 (hex) : Mode Control Word for Counter C0
76 (hex) : Mode Control Word for Counter C1
B6 (hex) : Mode Control Word for Counter C2

After writing the Mode Control Words, the counters can be loaded with the 16-bit count values. The Counters may be loaded in any order, but when a selected count register is to be loaded, it must be done with the least significant byte first followed by the most significant byte.

Each of the two USART devices need a Transmitter Clock input signal ($\overline{TxC}$) and a Receiver Clock input signal ($\overline{RxC}$), as explained later. The Baud rate generator device provides two clock signals CLOK1 and CLOK2, which may be connected to the $\overline{TxC}$ and $\overline{RxC}$ inputs of the two USARTs via a jumper pad. These clock signals may be divided by 1, 16 or 64 to derive the actual Baud rate, as specified in the mode instruction control word written into each USART during initialization. Table 7.9.3 specifies the values to be loaded into counters C1, C2 to generate different Baud rates. For best accuracy the ÷ 16 mode is recommended throughout.

The interval timer is realized via Counter C0 operating in Mode 2, with an input clock signal of 72 kHz. The timer signal $\overline{TCLK}$ will be low for one period of the input clock, and its period from one output pulse to the next equals the number of input counts in the count register. After the counter Mode setting during initialization, the timer signal $\overline{TCLK}$ will remain high until after the count register is loaded. If the counter register is reloaded between output pulses, the present period will not be affected, but the subsequent period will reflect the new value. Table 7.9.4 gives the required counter values for some typical time intervals.

BAUD RATE	COUNTER VALUES (HEX) FOR DIFFERENT FREQUENCY DIVISIONS WITHIN USART		
	÷ 1	÷ 16	÷ 64
9600	-	000F	0004
4800	01E0	001E	0008
2400	03C0	003C	000F
1200	0780	0078	001E
600	0F00	00F0	003C
300	1E00	01E0	0078
150	3C00	03C0	00F0
110	51D1	051D	0147
75	7800	0780	01E0

Notes:

1. All values are based on clock input at 2.304 MHz.
2. For errors less than 0.01%, use ÷ 16 mode throughout.
3. For Baud rates 9600 and 4800, ÷ 64 mode is not recommended due to the large error margin.

Table 7.9.3 : Counter Values for Different Baud Rates

INTERVAL TIME (msec)	COUNTER VALUE (HEX)
1	0048
10	02D0
100	1C20
500	8CA0
750	D2F0

Note: All values are based on clock input at 72 kHz

Table 7.9.4 : Counter Values for Typical Time Intervals

USART Devices for Channel 1 and 2

These Programmable Communications Interface devices can be programmed by the DCE software to operate using virtually any serial data transmission technique presently in use. They convert parallel format system data into serial format for transmission, and convert incoming serial format data into parallel data for reception. They delete or insert bits or characters that are functionally unique to the communication technique, and present a simple parallel input or output interface to the DCE-BUS.

Each of the two USART devices need a Transmitter Clock input signal $\overline{TxC}$, and a Receiver Clock input signal $\overline{RxC}$. The Transmitter Clock controls the rate at which the characters are to be trnasmitted. The Receiver Clock controls the rate at which the characters are to be received. The falling edge of $\overline{TxC}$ shifts the serial data out of the USART, while data is sampled into the USART on the rising edge of $\overline{RxC}$.

In Synchronous transmission mode, the frequencies of $\overline{TxC}$ and $\overline{RxC}$ signals are equal to the actual transmit and receive Baud rates respectively.

In Asynchronous transmission mode, the actual Baud rate can be software selected as ÷ 1, ÷ 16, or ÷ 64 of the Transmitter and Receiver Clock frequencies (usually ÷ 16 or ÷ 64).

The USART transmitter buffer accepts parallel data from the DCE-BUS Data Path, converts it into a serial bit stream, inserts the appropriate characters or bits based on the communication technique, and outputs a composite serial stream of data on the TxD output pin. The Transmitter Ready TxRDY output signal indicates that the transmitter is ready to accept a parallel data character. It can be used to generate a DCE

interrupt request, or it can be polled using a status read operation to the USART or the General Status Buffer. TxRDY is automatically reset when a transmit character is loaded into the USART.

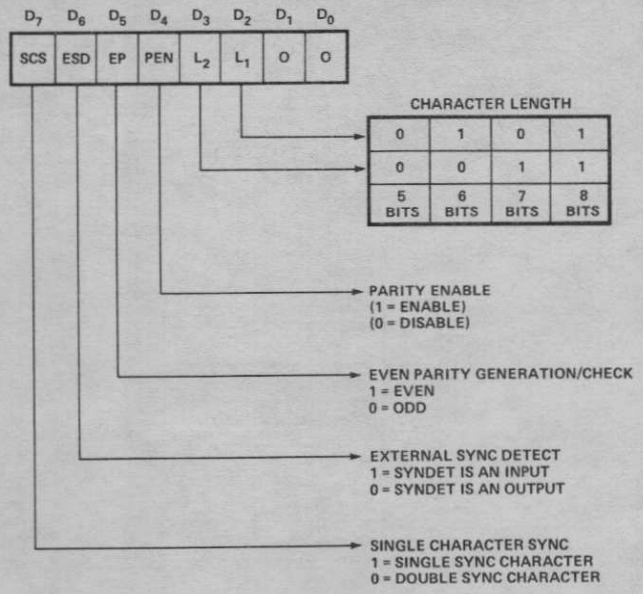
The USART receiver buffer accepts serial data from the RxD input pin, converts it into parallel format, checks for bits or characters unique to the communication technique, and sends the assembled data character to the DCE-BUS Data Path. The Receiver Ready RxRDY output signal indicates that the USART has received and assembled a data character ready for parallel input to the DCE-BUS. It can be used to generate a DCE interrupt request, or it can be polled using a status read operation to the USART or the General Status Buffer. RxRDY is automatically reset when the received character is read from the USART.

Different modes of communication between the internal registers of the two USART devices and the DCE-BUS Data Path are established, depending on the Card/Device address received by the RWC-CCE module from the DCE-BUS. Table 7.9.5 gives the addressing for both channels.

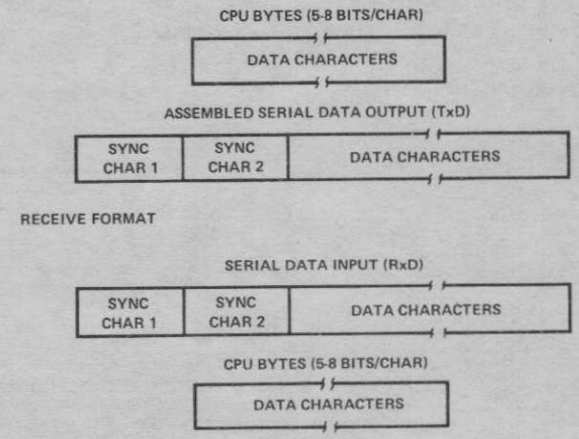
Prior to starting data transmission or reception, each USART must be loaded with a set of control words from DCE system software. These control signals determine the complete functional definition of the USART, and they must follow a Reset operation (internal or external). The control words are split into two formats:

- Mode Instruction
- Command Instruction

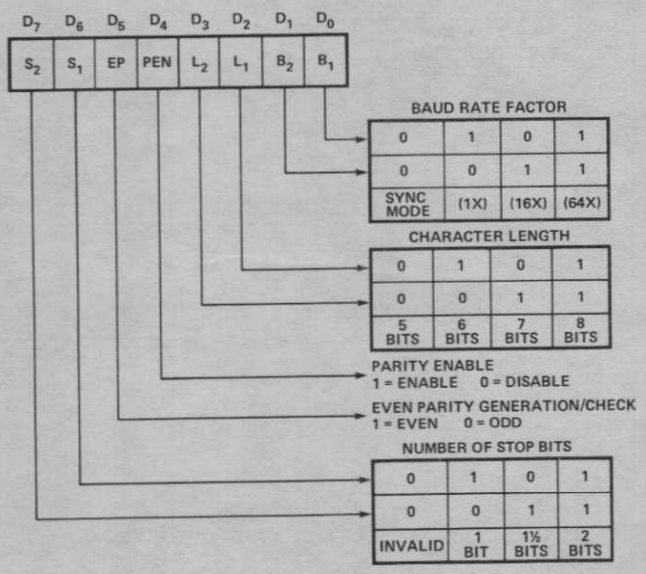
The Mode Instruction word defines the general operation characteristics of the USART. Once this has been written into the USART, SYNC characters or Command instructions may be inserted. It must follow a Reset operation.



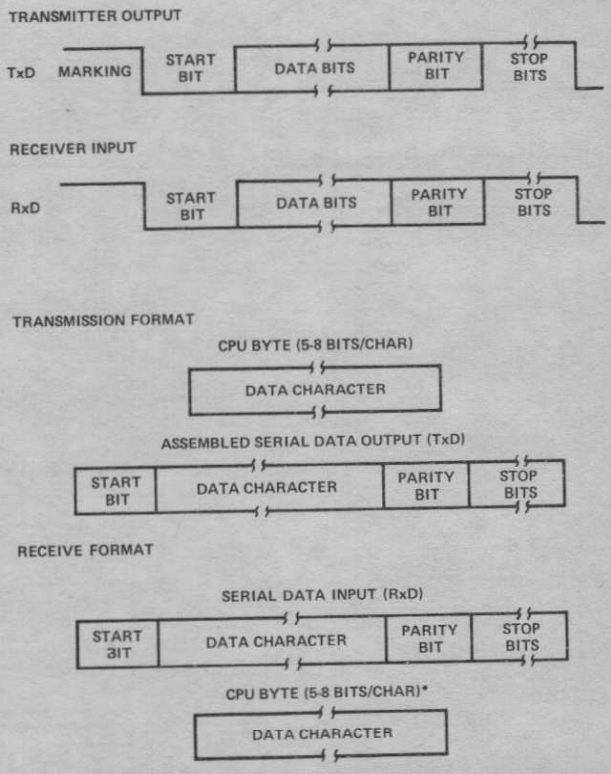
Mode Instruction Format, Synchronous Mode



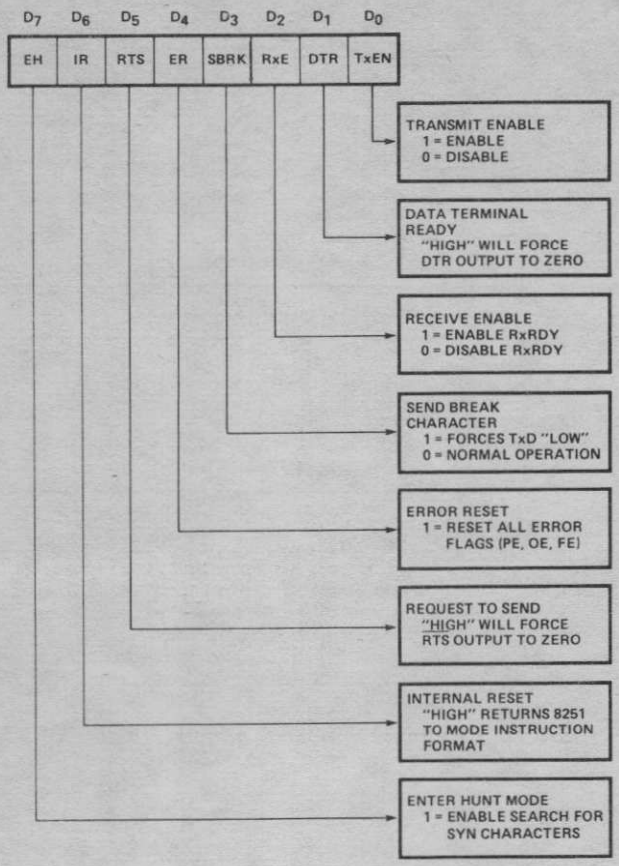
Synchronous Mode, Transmission Format



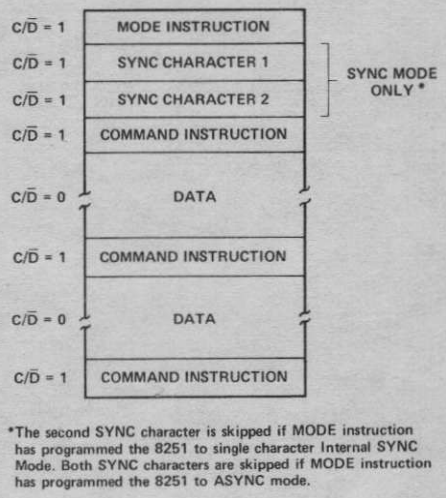
Mode Instruction Format, Asynchronous Mode



Asynchronous Mode

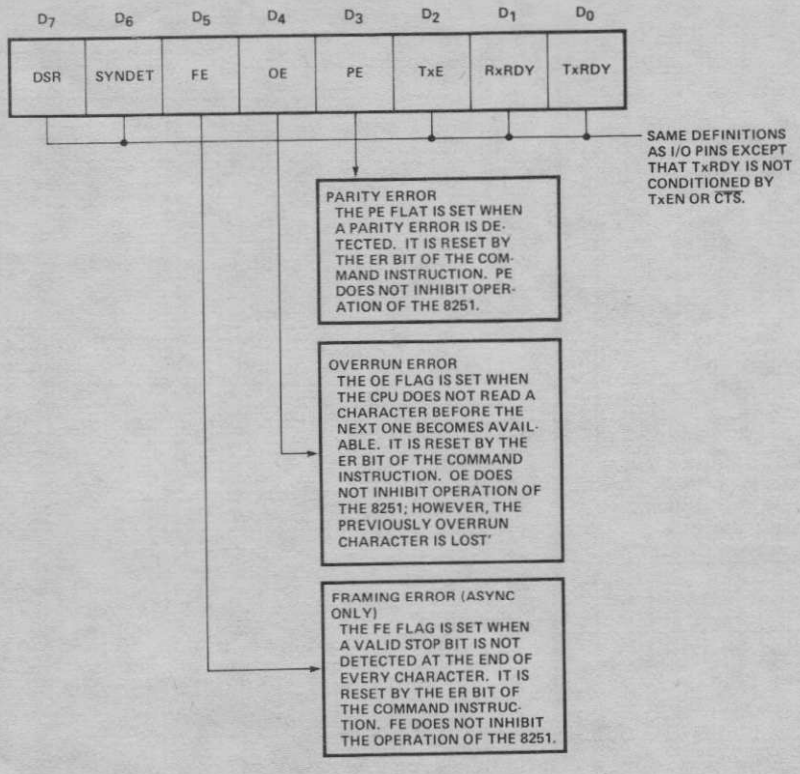


Command Instruction Format



*The second SYNC character is skipped if MODE instruction has programmed the 8251 to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the 8251 to ASYNC mode.

Typical Data Block



Status Register Format

Channel 1 USART Address (Hex)	Channel 2 USART Address (Hex)	$\overline{RD}$	$\overline{WR}$	OPERATION
Y4 or Y6	Y8 or YA	0	1	USART → DCE-BUS Data
Y4 or Y6	Y8 or YA	1	0	DCE-BUS Data → USART
Y5 or Y7	Y9 or YB	0	1	USART Status → DCE-BUS Data
Y5 or Y7	Y9 or YB	1	0	DCE-BUS Data → USART Control
any value except above	any value except above	X	X	3-State
XX	XX	1	1	3-State

Notes:

1. Y is the card address select switch setting in hex (1 to F)
2. X means don't care.
3. Bit 1 of the address is a don't care state.
4. RDRWC and WRRWC software routines provide the $\overline{RD}$ and $\overline{WR}$ signals accordingly.

Table 7.9.5 : USART Register Addressing for Channels 1 and 2

The Command Instruction word defines a format that is used to control the actual operation of the USART. All control words written into the USART after the Mode Instruction will be interpreted as Command Instructions (addressing for control words are Y5 or Y7, and Y9 or YB as shown in Table 7.9.5). Command Instruction words can be written into the USART at any time, even in the middle of data blocks. The Command Instruction controls the actual operation of the format selected by the Mode Instruction word. To return to the Mode Instruction state, a bit in the Command Instruction word can be set to initiate an internal Reset operation of the USART. Command Instructions must follow the Mode Instruction or SYNC characters (if in Synchronous Mode).

The internal status of each USART device can be read at any time during the functional operation. A normal Read sequence to the control word addresses (Y5 or Y7, Y9 or YB) will gate the USART status word into the DCE-BUS Data Path. Some of the bits in this Status word have identical meanings to external output pins, so that the USART devices can be polled or interrupt driven.

General Status Buffer

In addition to the status register within each USART, the RWC-CCE module has a General Status Buffer. It gates the following status condition signals on to the DCE-BUS Data Path when enabled:

b7 = RxRDY from Channel 1 USART
b6 = RxRDY from Channel 2 USART
b5 = TxRDY from Channel 1 USART
b4 = TxRDY from Channel 2 USART
b3 = Modem Clock failure on Channel 1
b2 = Modem Clock failure on Channel 2,
or
Interval Timer (Counter C0) time-out
b1, b0 = not used

The above 6 input status signals can be made to generate a common interrupt request to the DCE processor via a jumper option. Following such an interrupt, DCE software can strobe the General Status Buffer and determine the interrupt source with a single Read operation. Polled operation is also possible where the DCE software periodically scans the contents of the status buffer.

Status signals corresponding to bits 4 to 7 are reset by the USART devices, as explained earlier. Signals corresponding to bit 2 and 3 have to be reset by special Read operations to the General Status Buffer. Table 7.9.6 gives the addressing for the different operations associated with

the General Status Buffer signals.

ADDRESS (HEX)	$\overline{RD}$	OPERATION
YC	0	Read General Status Buffer
YD	0	Read General Status Buffer and reset Channel 1 modem clock failure signal
YE	0	Read General Status Buffer and reset Channel 2 modem clock failure signal, or, interval timer time-out signal
YF	0	combination of the operations for YD and YE.

Notes:

1. Y is the card address select switch setting in hex (1 to F).
2. It is not possible to read and reset a status signal by a single read operation (eg. a Read to YD must be preceded by a Read to YC).

Table 7.9.6 : General Status Buffer Addressing

Special Considerations

The Baud Rate Generator and Interval Timer device (8253) does not have a hardware reset input. Therefore changing the mode Control Word for a particular counter must be done after two successive dummy read operations (16-bit count value) to that counter, in order to clear the control logic on the device. A typical sequence for configuring and loading Counter 1 is as follows:

Select Control Word Register address (Y3).
Write Mode Control Word for Counter 1.
Select Counter 1 address (Y1).

Read Counter 1.
Read Counter 1.
Select Control Word Register address (Y3).
Write Mode Control Word for Counter 1.
Select Counter 1 address (Y1).
Load least significant byte of counter value.
Load most significant byte of counter value.

The USART devices cannot begin transmission until the Transmitter Enable bit TxEN is set in the Command Instruction, and a Clear To Send input $\overline{CTS}$ is received. In systems where $\overline{CTS}$ is not used, this line (pin 5) should be connected to +5V (pin 11). This equally applies to situations using the 20 mA current loop interface.

In order to enable the transmitter on a selected Channel the User must connect the 'Request to Send' output signal RTS available at pin 4 on that Device Connector, the 'Clear To Send' input signal CTS at pin 5. Bit 5 in the Command Instruction for that Channel must then be set, to make the RTS output active.

TxEN and $\overline{CTS}$ should remain asserted until the transmission is complete. Loss of either will immediately clamp the serial output line. They should remain active not only until the USART has completed the transfer of all bits of the last character, but also until they have cleared the modem. A delay of 1 msec following a proper occurence of TxE (USART status bit) is usually sufficient.

Extraneous transitions can occur on TxE becoming active, while data (including USART generated SYNs) is transferred to the parallel-to-serial converter. This situation can be avoided by ensuring that TxE occurs during several consecutive USART status read operations before assuming that the transmitter is truely in the empty state.

The TxRDY status bit and the TxRDY output signal are not functionally identical. Their definitions are as follows:

TxRDY status bit = Transmit buffer empty

TxRDY pin out = (Transmit buffer empty) & (CTS) & (TxEN)

When the USART is not transmitting, the TxRDY status bit will always be set. However, the TxRDY output will be high only if in addition, the TxEN bit in the Command Instruction is set and an active Clear To Send is received. Therefore in interrupt driven applications a continuous DCE interrupt request when the USART is not transmitting can be prevented by clearing bit TxEN in the Command Instruction.

Output of commands to the USART can destroy the integrity of a transmission in progress if timed incorrectly. This can normally be avoided by waiting for the USART status bit TxRDY to go high, indicating the end of the transmission. Status bit or signal TxRDY going high does not mean that the actual serial transmission is completed. Thus, for certain commands (e.g. software Reset), it is necessary to wait for TxE to go high. Status bit TxE is independent of the TxEN bit in the Command Instruction word.

In Synchronous mode, a 'high' on status bit TxE indicates that a character has not been loaded into the USART, and that the SYNC character or characters are about to be transmitted automatically as 'fillers'. TxE goes low as soon as the SYNC is being shifted out.

If the Interval Timer feature is required, pin 8 of the Channel 2 Device Connector should be connected to +5V.

RWC-CCE / DCE-BUS Protocol

Configure the Baud Rate Generator and Interval Timer device by writing the appropriate Mode Control Words for the three counters C0, C1, C2. Then load counters C1 and C2 with the 16-bit count values corresponding to the required Baud rates for Channel 1 and 2 respectively (see Table 7.9.3). When the Interval Timer feature is needed.

load counter C0 with the 16-bit count value corresponding to the time delay required (see Table 7.9.4). When loading the counters the least significant byte must always be loaded first, followed by the most significant byte.

Configure the USART device for each channel by writing the Mode Instruction word into the control register. For Synchronous mode this is followed by one or two SYNC characters. After that, write the Command Instruction word into the control register. The USART device is then ready for serial data reception and transmission. Since the same register address is used for both mode and command bytes, a condition may occur when the user does not know if the system will treat the next byte as a mode or command byte. In this circumstance the user should send the sequence Hex 92, Hex 77. This is a dummy mode/command byte followed by a software reset. The next byte sent by the user will be accepted as a mode definition. This reset sequence is recommended to be used at the initialisation of the card.

If the General Status Buffer signals are jumper connected to generate a common single interrupt request, the DCE interrupt service routine should read the General Status Buffer to determine the source of the interrupt, and then branch to the corresponding processing routine. Interrupts due to modem clock failure on Channels 1 or 2, or interval timer time-out, should be reset by a second read operation to the General Status Buffer with suitable bit settings. These two signals should be reset during initialization.
For polled operation, DCE software must read the General Status Buffer periodically and test the various status bits.

7.9.4.3 User Options

Interrupt Jumper Options

The 6 status signals at the General Status Buffer can be merged into a single DCE interrupt request signal. This signal may be jumper connected to IN7 or EXINTR on the DCE-BUS, by connecting jumpers 1-2 or 1-3 respectively. The module is delivered with jumpers 1-3 already installed.

The two status signals corresponding to the modem clock failure signals for channel 1, 2 and the interval timer time-out are also included in the interrupt generation scheme as shown on the block diagram in Section 7.9.3.

20mA Current Loop or V24 Interface Selection

Both Channels on the RWC-CCE module can be easily configured by the user for 20mA current loop or V24 interface. The serial data receive and transmit lines (RxD and TxD) can be switched between the two types of interface, simply by means of a hexadecimal switch located near the middle of the card. The table below summarizes the different settings on this switch.

Hexadecimal Switch Setting	Type of Interface for the RxD and TxD data lines	
	Channel 1	Channel 2
0	V24	V24
3	V24	20mA
C	20mA	V24
F	20mA	20mA

The jumper pads used for connecting the USART signals to the Device Connector pins for the two interface options are shown in the functional block diagram in Section 7.9.3. Links already installed when the module is delivered are also shown.

Jumper pads S3 and S4 enable the 20mA current loop interface signals to be brought out to the Device Connectors. These links are mounted on two separate component carriers for the two channels, soldered directly onto the card near the two Device Connectors. The module

is delivered with all the links installed on these two carriers.

Jumper pads S1 and S2 enable the V24 interface signals to be brought out to the Device Connectors. These links are mounted on two separate socket mounted component carriers for the two channels. They allow the user to independently select the internal Baud Rate Generator clock signal, or external signals for $\overline{\text{RxC}}$ and $\overline{\text{TxC}}$ clock inputs to the two USART devices. They also allow the Data Terminal Ready $\overline{\text{DTR}}$ output signal from each USART to be connected to Device Connector pin 20 when used with a Modem, or to pins 13, 14 for driving the reader controller when using a TTY. When used as a TTY reader controller, $\overline{\text{DTR}}$ low will activate the reader step relay. It will remain active until the time that a character is received by the communication channel.

At the Device Connector for the two communications channels, none of the 20mA current loop interface signal pins overlap with the V24 interface signal pins.

Transmitter Clock/Data Set Ready Select Jumpers

Jumper pads 4-5-6 and 7-8-9 allow one out of the two external input signals, Transmitter Clock (pin 15) or Data Set Ready (pin 6) to be selected for input to the USART devices. Linking 4-5 and 7-9 selects the Data Set Ready input signal for Channels 1 and 2 respectively. Linking 5-6 and 7-8 selects the external Transmitter Clock input signal for Channels 1 and 2 respectively.

Links 4-5 and 7-9 are already installed when the module is delivered.

Jumper pads 4-5-6 and 7-8-9 are related to links 6-11, 7-10, 8-9 on jumper pads S1 and S2 respectively, as shown in the block diagram in Section 7.9.3. These correlations must be maintained when changing jumper links on the module.

7.9.4.4 Module Connector Definitions

System Connector

See Section 6.1.4 for the pin definitions.

Device Connector

Two 25 pin D-type female connectors are installed on the module, one for each channel. They have the same pin definition:

Pin Number	Signal Name	Signal Mnemonic	Input/ Output
1	Chassis Ground	-	-
2	Transmit Data	TxD	O/P
3	Receive Data	RxD	I/P
4	Request to Send	RTS	O/P
5	Clear to Send	CTS	I/P
6	Data Set Ready	DSR	I/P
7	Signal Ground	-	-
8	Data Carrier Present	-	I/P
9	not used	-	-
10	not used	-	-
11	+5V supply	-	-
12	not used	-	-
13	- Reader Control	-RDC	O/P
14	+ Reader Control	+RDC	O/P
15	Transmitter Clock	TxC	I/P
16	+ Receive Data	+RxD	I/P
17	Receiver Clock	RxC	I/P
18	-5V supply	-	-
19	+ Transmit Data	+TxD	O/P
20	Data Terminal Ready	DTR	O/P
21	not used	-	-
22	- Receive Data	-RxD	I/P
23	not used	-	-
24	not used	-	-
25	- Transmit Data	-TxD	O/P

Chassis Ground connected to Signal Ground via 1mH choke.

Channel 1 connector is mounted on the component side of the circuit card. Pin 1 of each connector is the one nearest the outside edges of the card.

7.9.4.5 Interconnection of 2 RWC-CCE modules

In order to achieve communications over the maximum distance, the two systems may be interconnected by using the 20 mA loop and connecting +TXD to -RXD and -TXD to +RXD.
This provides twice the normal loop drive voltage that is available with only one card.

7.9.4.6 Operational Requirements

Signal Characteristics

The RWC-CCE module provides a user selectable V24 or 20 mA current loop interface on both channels. The V24 interface signals are in accordance with the recommended EIA Standard No. RS 232 C

Power Requirements

Typical current consumption values are as follows:

+5V : 300 mA
+12V : 100 mA
-5V : 35 mA

Environmental Requirements

Operating temperature : 0° C to 55° C
Storage temperature : -25° C to +85° C
Relative humidity : 95 % non-condensing

Bus Loading

The RWC-CCE module is equivalent to 4 unit loads on the DCE-BUS (see Section 4.4).

7.9.5 TEST PROCEDURE

This section defines a simple test configuration and a test program for performing a basic functional test on the RWC-CCE module. Users are advised to carry out such a test procedure when necessary to establish the correct functioning of a module. The test program also provides a good example of RWC-CCE module driver software.

Test configuration

The following test program tests Channel 1 of the RWC-CCE module. Connect a TTY to the Channel 1 device connector (mounted on the component side of the card). The program can be easily modified to test Channel 2 as well.

```
DAI 8080 ASSEMBLY SERVICE, D2.2


                        ; THIS IS A SIMPLE PROGRAM FOR TESTING THE
                        ; STANDARD RWC-CCE MODULE WITH CARD ADDRESS
                        ; SELECT SWITCH SET TO 'A'.  IT INITIALISES
                        ; CHANNEL 1, WAITS FOR CHARACTER INPUT
                        ; FROM A TTY CONNECTED TO CHANNEL 1, AND
                        ; THEN ECHOES BACK EACH INPUT CHARACTER
                        ; THROUGH THE TRANSMIT SIDE OF CHANNEL 1.
                        ; PROGRAM IS ENTERED FROM THE DCE UTILITY
                        ; BY A 'GO' COMMAND.  THE TTY CAN THEN BE
                        ; DISCONNECTED FROM THE ICB-ASR33 CABLE, AND
                        ; THEN RECONNECTED TO THE DEVICE CONNECTOR
                        ; FOR CHANNEL 1 OF THE RWC-CCE MODULE.

                        ; DEVELOPED USING DAI'S DISKETTE DEVELOPMENT SYSTEM
                        ; EDITOR AND MACRO ASSEMBLER HAVE BEEN
                        ; USED IN THIS DEVELOPMENT.
                        ;
                        ; ENSURE THAT CH1 CTS LINE IS CONNECTED TO +5V.
                        ;
031E            RDRWC   EQU     031EH
0349            WRRWC   EQU     0349H   ; DEFINE READ AND WRITE
                                        ; ROUTINE ADDRESSES.

                        ; THE FOLLOWING MACRO DEFINES
                        ; STGI FOR DCE-1 AND DCE-2 MODULES.

                STGI    MACRO   PORT

                        STA     01C00H+PORT

                        ENDM
```

```
1000                    ORG     1000H

                BEGIN:
1000 CD2110             CALL    INIT    ; INITIALISE CH1 USART
1003 CD3B10             CALL    BAUD    ; INITIALISE BAUD RATE
                                        ;       GENERATOR.
                LOOP:
1006 3EAC               MVI     A,0ACH  ; SELECT GENERAL STATUS
             +          STGI    1       ;         BUFFER.
1008 32011C

                WAIT:
100B CD1E03             CALL    RDRWC   ; READ BUFFER
100E E680               ANI     080H    ; RECEIVER READY?
1010 CA0B10             JZ      WAIT    ; IF NOT THEN WAIT

1013 3EA4               MVI     A,0A4H  ; SELECT CH1 DATA

             +          STGI    1
1015 32011C

1018 CD1E03             CALL    RDRWC   ; READ INPUT CHARACTER
101B CD4903             CALL    WRRWC   ; ECHO BACK

101E C30610             JMP     LOOP

                        ; INITIALISE CHANNEL 1 USART FOR
                        ; OPERATION WITH STANDARD TTY
                        ; (DIVIDE BY 16).

                INIT:
1021 3EA5               MVI     A,0A5H  ; SELECT USART CONTROL
             +          STGI    1       ;       REGISTER
1023 32011C

1026 3E92               MVI     A,092H  ; DUMMY MODE INSTRUCTION
1028 CD4903             CALL    WRRWC   ; ENSURES THAT FOLLOWING
                                        ; RESET COMMAND SYNCHRONISES
102B 3E77               MVI     A,077H  ; THE SET-UP OF THE
102D CD4903             CALL    WRRWC   ; USART.

1030 3ECE               MVI     A,0CEH  ; WRITE MODE INSTRUCTION
1032 CD4903             CALL    WRRWC

1035 3E37               MVI     A,037H  ; WRITE COMMAND INSTRUCTION
1037 CD4903             CALL    WRRWC

103A C9                 RET
```

```
                        ; INITIALISE BAUD RATE GENERATOR FOR CH1
                        ; 110 BAUD (DIVIDE BY 16).

                BAUD:
103B 3EA3               MVI     A,0A3H  ; SELECT CONTROL REGISTER
             +          STGI    1
103D 32011C

1040 3E76               MVI     A,076H  ; MODE CONTROL WORD FOR C1
1042 CD4903             CALL    WRRWC

1045 3EA1               MVI     A,0A1H  ; SELECT C1
             +          STGI    1
1047 32011C



104A CD1E03             CALL    RDRWC   ; TWO DUMMY READS
104D CD1E03             CALL    RDRWC   ; TO CLEAR COUNTER.

1050 3EA3               MVI     A,0A3H  ; SELECT CONTROL REGISTER
             +          STGI    1
1052 32011C

1055 3E76               MVI     A,076H  ; MODE CONTROL WORD
1057 CD4903             CALL    WRRWC   ; FOR C1.

105A 3EA1               MVI     A,0A1H  ; SELECT C1
             +          STGI    1
105C 32011C

105F 3E1D               MVI     A,01DH  ; LOAD LSB OF COUNT
1061 CD4903             CALL    WRRWC   ;      FOR 110 BAUDS.
1064 3E05               MVI     A,005H  ; LOAD MSB OF COUNT
1066 CD4903             CALL    WRRWC   ;      FOR 110 BAUDS.

1069 C9                 RET


0000                    END
```

```
BAUD  103B      BEGIN 1000      INIT  1021      LOOP  1006
RDRWC 031E      STGI  4FE7      WAIT  100B      WRRWC 0349
```

7.9.6 ORDERING INFORMATION

RWC-CCE : Standard Version.
Delivered with jumper links connected as shown on the block diagram in section 7.9.3.

7.10 RWC-SLD : SERIAL LINE DISTRIBUTOR

7.10.1 FUNCTIONAL DESCRIPTION

The RWC-SLD Real-World interface module enables the monitoring and distribution of up to 8 current mode serial communication channels (eg. telex lines), without interaction or interference with channel operation. Serial to parallel conversion of data is performed by DCE software.

Several RWC-SLD modules can be connected in parallel for independent, simultaneous, parallel distribution of each serial input channel to several terminal devices or other destinations.

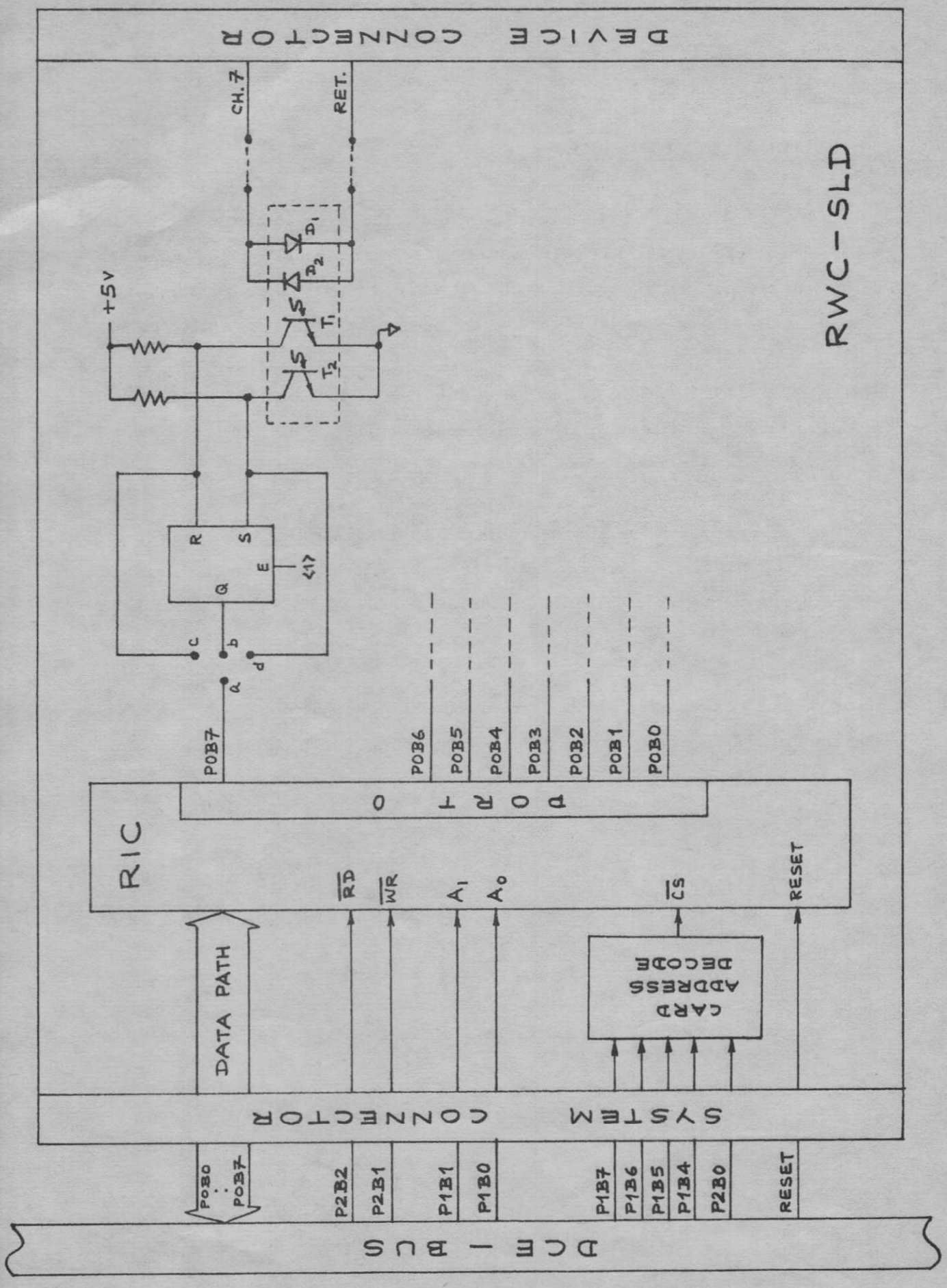
Each input channel is read via bipolar opto-isolated Schmitt trigger inputs, for complete isolation with no interference. Line termination resistor sockets are provided to allow user selectable load impedences for each channel.

Each module has an identification address defined by a hexadecimal switch, and up to fifteen modules can be directly connected to the DCE-BUS.

7.10.2 FEATURES

- monitors up to 8 current mode serial communication channels.
- capability for independent, simultaneous, parallel distribution of each serial input channel to several different destinations.
- bipolar opto-isolated Schmitt trigger inputs for complete channel isolation.
- sockets for line termination resistors to allow user selectable channel load impedences.
- standard hardware and software interface to the DCE-BUS.
- selectable module address.
- single 100 x 160 mm eurocard format.

7.10.3 FUNCTIONAL BLOCK DIAGRAM



7.10.4 SYSTEM DESIGN PARAMETERS

7.10.4.1 Hardware Configuration

The functional block diagram in Section 7.10.3 illustrates the hardware configuration of the RWC-SLD module. It has the standard RIC interface to the DCE-BUS.

Each pair of serial input channel lines is read via bipolar opto-isolators. The two signal outputs from each opto-isolator are connected to a R/S latch. The latched output can be jumper connected to one of the lines of RIC Port 0 programmed in input mode. Each data line of RIC Port 0 can also be jumper connected to either or both of the two digital signals from the opto-isolator for that channel.

The eight lines of RIC Port 0 can thus be individually jumper configured to read any one of the following conditions associated with its corresponding channel :

- last detected current direction (latched)
- detection of forward current
- detection of reverse current
- detection of current or no-current in either direction.

The serial to parallel conversion of data for each channel can be done by DCE software.

Any of the eight input serial communication channels can be safely distributed to several destinations, by parallel connection to a selected channel input on each member of a group of RWC-SLD modules. Such a scheme can be used to realize fail-safe systems where critical messages have to be distributed in parallel to several destinations.

DEVICE ADDRESS (HEX)	$\overline{RD}$	$\overline{WR}$	OPERATION
INP Y0	0	1	RIC Port 0 → DCE Data Bus
Y1	0	1	Not applicable
Y2	0	1	Not applicable
Y3	0	1	Illegal Condition
Y0	1	0	Not applicable
Y1	1	0	Not applicable
Y2	1	0	Not applicable
OUT Y3	1	0	DCE Data Bus → RIC Command Register
ZX	X	X	RIC Data Bus in 3-state

Notes:

1. Y is the card address select switch setting in hex.
2. Z is any number other than Y.
3. X means don't care.
4. Bits 2 and 3 in the low-order byte of the Device Addresses are don't care states.
5. RDRWC and WRRWC software routines provide the $\overline{RD}$ and $\overline{WR}$ signals accordingly.

Table 7.10.1 : Device Address Table for RWC-SLD

7.10.4.2 Programming Specifications

The RWC-SLD module is addressed via the standard DCE-BUS interface. Programming specifications for driving the DCE-BUS are given in Section 4.1.

RIC Device Addresses

The RIC on the RWC-SLD module has 3 data ports and a command register. Different modes of communication between the RIC registers and the DCE-BUS Data Path are established depending on the Device Address received by the RWC-SLD module from the DCE-BUS. Table 7.10.1 shows the Device Addresses applicable to RWC-SLD operation.

RIC Configuration

Port 0 of the RWC-SLD module RIC must be configured in input mode. Ports 1 and 2 are not used. The RIC should be initialized by writing to the RIC command register any control word which configures Port 0 as input (eg. 9BH).

Format and Interpretation of Data

The status of the eight input channels are read by DCE software via Bits 0 - 7 of RIC Port 0. Bits 0 to 7 are associated with channels 0 to 7 respectively.

The interpretation of each data bit corresponding to each of the input channels depends on the jumper configuration for that input signal line. The interpretation of each bit is given below for different configurations of the associated jumper network a-b-c-d (see Section 7.10.3) :

a-b : 0 = last detected current in forward direction
1 = last detected current in reverse direction

a-c : 0 = forward current
1 = no forward current

a-d : 0 = reverse current
1 = no reverse current

a-c-d : 0 = current in either forward or reverse direction
1 = no current in either direction

Each of the eight input signals is connected to jumper pad 'a' in the associated jumper network. See Section 7.10.4.3 for actual values corresponding to a, b, c, d for the eight different input signals. Forward current is defined as current flowing towards the return wire.

.10.4.3 User Options

Input Signal Jumpers

Each of the 8 input lines to RIC Port 0 is routed through a separate jumper network a-b-c-d, as shown in the block diagram in Section 7.10.3. Table 7.10.2 gives the actual values of these jumper pads for each of the eight channels. The RWC-SLD module is usually delivered with jumper links 13-2, 14-5, 15-8, 16-11, 29-18, 30-21, 31-24, 32-27 already installed.

Termination Resistors

Each pair of input channel lines are routed via sockets provided for the insertion of connection links or termination resistors mounted on component carriers.

Table 7.10.2 shows the relationship between the input channel number

and the required links on the two 16-pin sockets marked 'A' and 'B' on the module.

Serial termination resistors should be installed where necessary to achieve correct switching currents at the input diodes of the opto-isolators. The actual values of the resistors will depend on the characteristics of the corresponding serial input channels.

The RWC-SLD module is usually delivered with connecting links installed on component carriers.

Input Channel No.	Port 0 Bit No.	Termination Links		Jumper Pad a	b	c	d
0	0	B7-B10,	B8-B9	32	27	26	28
1	1	B5-B12,	B6-B11	31	24	23	25
2	2	B3-B14,	B4-B13	30	21	22	20
3	3	B1-B16,	B2-B15	29	18	19	17
4	4	A7-A10,	A8-A9	16	11	10	12
5	5	A5-A12,	A6-A11	15	8	7	9
6	6	A3-A14,	A4-A13	14	5	6	4
7	7	A1-A16,	A2-A15	13	2	3	1

Table 7.10.2 : Jumper Pad and Termination Definitions for the Eight Input Channels

7.10.4.4 Module Connector Definitions

System Connector

See Section 6.1.1 for the pin definitions.

Device Connector

Pin definitions for the 25-pin D-type female device connector are as follows :

Pin Number	Signal
1	Channel 1
2	" Return
3	Channel 2
4	" Return
5	Channel 3
6	" Return
7	Channel 4
8	" Return
9	Channel 5
10	" Return
11	Channel 6
12	" Return
13	Channel 7
25	" Return
14	Channel 0
15	" Return
16 - 24	Ground

7.10.4.5 Operational Requirements

Opto-Isolator Input Diode Ratings

Logic states	:	Logic ONE > 2mA
	:	Logic ZERO < 100µA
Max. continuous forward current	:	60mA
Peak reverse current	:	10µA
Max. reverse voltage	:	3V
Rated forward voltage at 20mA	:	1.25V typical at 25°C
Min. isolation	:	500V

Power Requirements

The RWC-SLD module uses a single +5 volt supply. Typical power consumption is 90mA.

Environmental Requirements

Operating temperature	:	0°C to 55°C
Storage temperature	:	-25°C to +85°C
Relative humidity	:	95% non condensing (isolation may be reduced with high humidity)

Bus Loading

The RWC-SLD module presents 1 unit-load to the DCE-BUS (see Section 4.4).

7.10.5 ORDERING INFORMATION

RWC-SLD : Standard Version
includes component carriers with connection links.