7.7 RWC-V8/16 : HIGH-SPEED ANALOG DATA ACQUISITION

7.7.1 FUNCTIONAL DESCRIPTION

The RWC-V8/16 Real-World interface module provides a low-cost interface between a DCE Processor and the SDM853 Burr-Brown data acquisition module. Sockets are provided for mounting the SDM853 module, and the Burr-Brown model 546 dual power supply module.

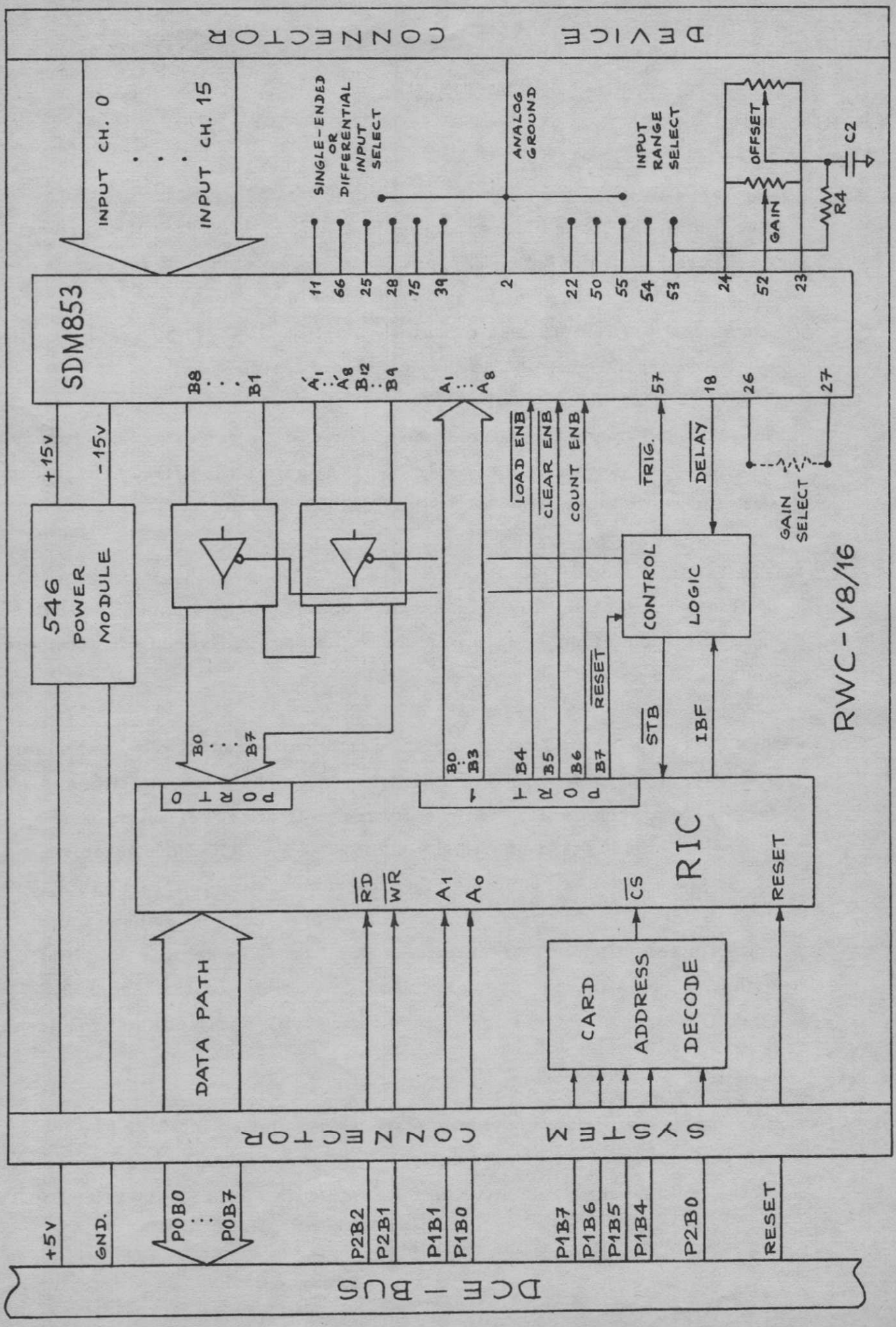
The SDM853 module accepts either 16 single-ended or 8 differential multiplexed analog inputs, and converts into 12-bit digital words with an accuracy of $\pm$ 0.025%. Input signal ranges of $\pm$ 10mV to $\pm$ 10V permit direct connection to many common signal sources including low level sensors such as thermocouples and strain gauges.

Each RWC-V8/16 card has an identification address defined by a hexadecimal switch, and up to fifteen cards may be connected to the DCE-BUS.

7.7.2 FEATURES

- 16 single-ended or 8 differential analog inputs.
- input signal ranges from $\pm$ 10mV to $\pm$ 10V.
- resolutions of 2.4μV to 2.4mV (12 bit).
- 0.025% full scale range accuracy at unity gain.
- includes Sample and Hold amplifier.
- includes instrumentation amplifier for common-mode rejection and high gain.
- gain selectable from 1 to 1000.
- random or automatic increment channel selection modes.
- up to 25,000 samples per second into the DCE system.
- uses standard DCE power supplies.
- standard hardware and software interface to the DCE-BUS.
- selectable card address.
- single 100 x 160 mm eurocard format.

7.7.3 FUNCTIONAL BLOCK DIAGRAM



7.7.4 SYSTEM DESIGN PARAMETERS

7.7.4.1 Hardware Configuration

The functional block diagram in Section 7.7.3 illustrates the hardware configuration of the RWC-V8/16 module. The standard version is supplied without the two Burr-Brown modules. It has sockets provided for easy insertion of these modules. Option OPT 001 is supplied with the two Burr-Brown modules installed and tested.

The SDM853 module provides many user options via external jumpers. The relevant jumper points are made available on the RWC-V8/16 card, with the same numbering as on the SDM853 module.

The SDM853 module has two one-of-eight analog multiplexers, providing user selection of 16 single-ended or 8 double-ended channels by external jumpers. The RWC-V8/16 module is jumper configured for 16 single-ended input operation, when delivered.

The RWC-V8/16 module can be software configured to accept random addresses, or to sequence through all analog channels on command from a trigger generated from software. Channel selection is by a 3 or 4-bit binary word provided via Bits 0 - 3 of RIC Port 1, or via a presettable address counter. The instrumentation amplifier is a low drift differential amplifier featuring high speed at gains above unity, and gain selection with an external resistor. The card is supplied without a resistor, giving a gain of 1. At gains greater than 100, effective input offset voltage is less than 400μV with voltage drift less than 2μV/°C.

The analog-to-digital converter features resolution of 12 binary bits, external gain and offset adjustment, unipolar straight binary or bipolar offset binary output. It may be operated with jumper selectable input

voltage ranges of 0 to +5, 0 to +10, -2.5 to +2.5, -5 to +5, and -10 to +10 volts after the amplifier gain. The module is delivered with the input range -10 to +10 volts jumper selected.

7.7.4.2 Programming Specifications

The RWC-V8/16 module is addressed via the standard DCE-BUS interface. Programming specifications for driving the DCE-BUS are given in Section 4.1.

RIC Initialization

The RIC on the RWC-V8/16 module should be initialized by writing the control word 0B0H to the RIC Command Register. This configures RIC Port 0 as handshaking input and RIC Port 1 as output. RIC Port 0 is used for reading the digital result of a conversion, as well as the channel address output. The unused bits of Port 2 are not relevant.

RIC Device Addresses

The RIC on the RWC-V8/16 has 3 data ports and a command register. Different modes of communication between the RIC Ports and the DCE-BUS data path are established depending on the Device Address received by the RWC-V8/16 module from the DCE-BUS. Table 7.7.1 shows the Device Addresses needed for different communication modes.

DEVICE ADDRESS (HEX)	$\overline{RD}$	$\overline{WR}$	OPERATION
Y0	0	1	RIC Port 0 → DCE Data Bus
Y1	0	1	Invalid Operation
Y2	0	1	Invalid Operation
Y3	0	1	Illegal Condition
Y0	1	0	Invalid Operation
Y1	1	0	DCE Data Bus → RIC Port 1
Y2	1	0	Invalid Operation
Y3	1	0	DCE Data Bus → RIC Command Register
ZX	X	X	RIC Data Bus in 3-state

Notes:

1. Y is the card address select switch setting in hex (1 to F).
2. Z is any number other than Y.
3. X means don't care.
4. RDRWC and WRRWC software routines provide the $\overline{RD}$ and $\overline{WR}$ signals accordingly.
5. Bits 2 and 3 in low-order byte of the Device Addresses are don't care states.

Table 7.7.1 : Device Address Table for RWC-V8/16

Format of Data

The digital output from the SDM853 module corresponding to a selected analog input signal, is input to the DCE-BUS via RIC Port 0. The digital result from the converter consists of 12 bits. These 12 bits and the 4 channel address output bits are read by two successive Read operations to RIC Port 0.

Input signal allocation for the two successive Read operations are as follows:

Port 0 : b0 = channel address bit A0
b1 = A1
b2 = A2
b3 = A3
b4 = digital output data bit B0 (LSB)
b5 = B1
b6 = B2
b7 = B3

b0-b7 = digital output data bits B4-B11 (MSB)

Note: In the SDM853 documentation from Burr-Brown the above channel address bits A0, A1, A2, A3 are referred to as A1, A2, A4, A8 and the digital output data bits B0 to B11 are referred to as LSB12 to MSB1 respectively.

The input channel select address (for random channel selection) and 4 control signals are sent from the DCE-BUS to RIC Port 1. Signal allocation is as follows:

Port 1 : b0 - b3 = channel select address A0 - A3
b4 = $\overline{\text{LOAD ENB}}$ (load enable)
b5 = $\overline{\text{CLEAR ENB}}$ (clear enable)
b6 = COUNT ENB (count enable)
b7 = $\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ signal is used during initialization to ensure correct sequence of data input during the successive Read operations to RIC Port 0. It is normally held in the inactive 'high' state.

$\overline{\text{LOAD ENB}}$, $\overline{\text{CLEAR ENB}}$ and COUNT ENB signals control the channel address selection at the analog multiplexer. They become effective as a conversion is triggered, and set the channel select address for the following conversion. $\overline{\text{LOAD ENB}}$ loads the channel address from RIC Port 1 Bits 0 - 3, and is used for random channel selection. $\overline{\text{CLEAR ENB}}$ sets the channel address to zero. It has the same effect as loading address zero via RIC Port 1 Bits 0 - 3. COUNT ENB enables address incrementing at each conversion, thus allowing automatic cycling of all the analog input channels. Only one of these three control lines should be active at any one time.

Interpretation of Data

The 4-bit channel address read from RIC Port 0, along with the 4 low bits of the digital result, is applicable only for the following conversion. This address is therefore one step ahead of the current digital result read along with it.

The A/D converter on the RWC-V8/16 module gives a 12-bit digital result in unipolar straight binary or bipolar offset binary. The digital results corresponding to input values equal to the upper and lower limits of the selected input range is 12 zeroes and 12 ones respectively. This holds true for unipolar as well as bipolar input ranges. This is illustrated in

the examples below:

ANALOG INPUT			12-BIT DIGITAL OUTPUT
+2.5	+10	⟶	000000000000
.	.		.
.	.		.
.	.		.
0	+5	⟶	011111111111 100000000000
.	.		.
.	.		.
.	.		.
-2.5	0	⟶	111111111111

The digital output can be interpreted to suit specific requirements. For example, by complementing all but the most significant bit by software the result will be in two's complement form suitable for performing arithmetic operations etc. where a sign capability is needed.

Special Considerations

The RWC-V8/16 module uses RIC Port 0 configured in handshake input mode, for reading all the digital output data from the SDM853 module. The handshake control signals $\overline{STB}$ and IBF are used also to trigger the next conversion.

The sequence of operation for the RWC-V8/16 module is given below. Only steps (a) and (e) are directly related to the associated software.

a) DCE software reads the channel address currently latched at the multiplexer, and the low order four bits of the result from the last completed conversion, from RIC Port 0.

b) The high order eight bits of the digital result are automatically latched into RIC Port 0, as a consequence of step (a).

c) The next conversion is automatically triggered, as a consequence of step (a). The selected channel is the one whose address has already been latched into the analog multiplexer during the execution of step (d) in the previous cycle. This is the channel address read at step (a).

The channel address read during step (a) is therefore one step ahead of the converted digital result. The converted digital result for this channel address will be read during step (a) of the next cycle.

d) A new channel select address is latched into the analog multiplexer, as a consequence of step (c). Channel address selection depends on the status of the control signals $\overline{\text{LOAD ENB}}$, $\overline{\text{CLEAR ENB}}$ and COUNT ENB before execution of step (a). Since step (c) has already triggered a conversion, the latched new address is only applicable for the following conversion.

e) DCE Software reads the high order eight bits of the converted digital result from RIC Port 0. This data has been latched at step (b).

f) At the end of the conversion triggered at step (c), the channel address latched into the analog multiplexer at step (d), and the low order four bits of the digital result are automatically latched into RIC Port 0.

g) Step (a) of the next operation cycle.

The two read operations (steps (a) and (e)) constituting each cycle must always be completed in order to maintain correct synchronization of low and high order data.

If analog inputs are to be read at random, the address of the next required channel and an active $\overline{\text{LOAD ENB}}$ signal must be present at RIC Port 1, before step (a) of a cycle. The converted digital output for this channel can be read back during the third cycle following the setting up of its address at RIC Port 1. The cycle immediately following the setting up of the channel address (say 'C') at RIC Port 1, will cause this address 'C' to be latched into the analog multiplexer ready for the next conversion. It will also trigger the conversion of the channel whose address was already in the latch (ie. which was latched during the previous cycle). The next cycle will trigger the conversion of channel 'C'. At the end of the conversion, the digital result will be automatically latched into RIC Port 0. The following cycle will read this digital result corresponding to channel 'C'.

A new conversion is triggered at step (a) by the act of reading the low order part of the digital result from the previous conversion. A long delay before the reading of the result of this new conversion could possibly mean that the result read is obsolete.

It is essential to have a minimum software cycle time between two successive read operations to RIC Port 0 for the low order bits of the digital result (step (a)). This is necessary to allow for the settling time of the multiplexer, amplifier, and sample and hold circuits, as well as the A/D conversion time. Since the instrumentation amplifier requires a longer settling time at high gains, the required delay increases with the gain. Table 7.7.2 shows the required minimum software cycle times for different gain values.

For normal software controlled read operations via subroutine RDRWC these minimum cycle times do not pose any problem at all, since each 'CALL RDRWC' instruction takes 146 μsec to execute. For fast systems implemented via the DCE-LSA module, it may be necessary to wait between successive cycles.

System Gain	System Accuracy	Throughput Rate (Channels/sec)	Minimum Software Cycle Time (µsec)
1	± 0.025%	25,000	40
10	± 0.035%	25,000	40
100	± 0.08%	25,000	40
1000	± 0.1%	12,500	80

Table 7.7.2 : System Performance (typical at 25°C)

RWC-V8/16 RIC / DCE-BUS Protocol

Initialization

The RWC-V8/16 module RIC should first be initialized by writing control word 0B0H to its Command Register. This will configure RIC Ports 0 and 1 as required.

Select a suitable combination of the control signals $\overline{\text{LOAD ENB}}$, $\overline{\text{CLEAR ENB}}$ and COUNT ENB, a channel address (if $\overline{\text{LOAD ENB}}$ is active), active $\overline{\text{RESET}}$ (Bit 7 = 0), and write the resulting control word to RIC Port 1.

Remove the Reset by setting Bit 7 = 1 in the above control word while keeping the other bits unchanged, and write again to RIC Port 1.

The RWC-V8/16 module logic is now ready for an analog to digital conversion.

A/D Conversion with Random Channel Selection

In the above control word written to RIC Port 1, set Bits 0-3 equal to the required channel address (say 'A'), and set $\overline{\text{LOAD ENB}}$ (Bit 4) active (control word = 0AAH). Then perform a dummy cycle via two Read operations to RIC Port 0. This will trigger a dummy conversion and latch the new channel address (A) ready for the following conversion. Write the next channel address (say 'B') to RIC Port 1 and then perform another dummy cycle via two Read operations to RIC Port 0. This will trigger the conversion of channel 'A' and latch channel address 'B' ready for the next conversion. The next channel address (say 'C') can then be written to RIC Port 1. The next two Read operations to RIC Port 0 will read the digital result corresponding to channel 'A' along with channel address 'B', trigger the conversion of channel 'B', and latch channel address 'C' for the next conversion.

The complete software sequence for the above example, assuming card address select switch set to 1, is given below:

```
MVI     A,13H       select RIC Command Register.
STGI    1
MVI     A,0B0H      configure the RIC ports.
CALL    WRRWC
MVI     A,11H       select RIC Port 1.
STGI    1
MVI     A,2AH       set up channel address 'A' and active
                    LOAD ENB, RESET.
CALL    WRRWC
MVI     A,0AAH      disable RESET.
CALL    WRRWC
                    ++ end of module initialization ++
```

```
MVI     A,10H       select RIC Port 0.
STGI    1
CALL    RDRWC       dummy cycle to trigger a dummy
                    conversion and latch channel address 'A'.
CALL    RDRWC
MVI     A,11H       select RIC Port 1.
STGI    1
MVI     A,0ABH      select channel 'B' for next conversion.
CALL    WRRWC
MVI     A,10H       select RIC Port 0.
STGI    1
CALL    RDRWC       trigger conversion of channel 'A' and
                    latch channel address 'B'.
CALL    RDRWC
CALL    RDRWC       read low-order part of result for channel
                    'A' and channel address 'B'; also trigger
                    conversion of channel 'B'.
store data
CALL    RDRWC       read high-order part of result for channel
                    'A'.
  .
  .
  .
```

A/D Conversion with Automatic Channel Address Increment

In the control word written to RIC Port 1 during initialization, set Bits 0-3 equal to the starting channel address (say '7'), and set COUNT ENB active (control word = 0F7H). The sequence of operation is similar to that for random selection of channels, except for the setting up of the next channel address at RIC Port 1 before each cycle. The channel address will be automatically incremented with the triggering of each conversion.

The software sequence for the above example, assuming card address select switch set to 1, is given below:

```
initialization
    .
    .
    .
MVI     A,11H       select RIC Port 1.
STGI    1
MVI     A,0F7H      set up starting channel address '7' and
                    active  COUNT ENB.
CALL    WRRWC
MVI     A,10H       select RIC Port 0
STGI    1
CALL    RDRWC       trigger a dummy conversion and latch
                    channel address '7'.
CALL    RDRWC
CALL    RDRWC       trigger conversion of channel '7' and
                    increment channel address to '8'.
CALL    RDRWC
CALL    RDRWC       read low-order part of result for channel
                    '7' and channel address '8'; trigger
                    conversion of channel '8' and increment
                    channel address to '9'.
store data
CALL    RDRWC       read high-order part of result for
                    channel '7'
    .
    .
    .
```

7.7.4.3 User Options

The SDM853 module provides many user options via external jumpers. The relevant jumper points are made available on the RWC-V8/16 card, with the same numbering as on the SDM853 module.

Input Type

The SDM853 module has two one-of-eight analog multiplexers, providing user selection of 16 single-ended or 8 differential input channels by

external jumpers at points 11, 66, 25, 28, 75, 2 (analog ground), 39 (digital ground).

For single-ended inputs with local ground connect pads 11-66-25, 28-2. Unused inputs should be grounded.

For differential inputs connect pads 75-39, 11-25, 66-28.

The RWC-V8/16 module is usually supplied with the single-ended input selection jumpers already installed.

Input Range

The input range for the A/D converter, after the instrumentation amplifier gain, can be selected via jumper pads 22, 50, 53, 54, 55, 2 (analog ground). The actual range will thus depend on the selected jumper configuration as well as the selected amplifier gain.

A/D Converter Input Range (V)	Jumper Links
0 to +5	53-55, 22-50, 54-2
0 to +10	22-50, 54-2, 55 open
-2.5 to +2.5	53-55, 22-50, 54-53
-5 to +5	53-54, 22-50, 55 open
-10 to +10	53-54, 55-50, 22 open

Pad 2 (analog ground) is also made available near the jumper pad group 22, 55, 54, 53, 50, for ease of connection.

The RWC-V8/16 module is usually supplied with the -10 to +10 volt range selection jumpers already installed.

Amplifier Gain

By connecting a suitable resistor between pads 26 and 27, the user can control the gain of the instrumentation amplifier over the range 1 - 1000.

The gain (G) obtained with an external resistance of R Ω is given by the formula:

$$G = 1 + 20k\Omega / R$$

An external resistor of 0.1% precision and a maximum temperature coefficient of $\pm$ 10 ppm/°C should be used.

The RWC-V8/16 module is usually supplied without a resistor, thus giving a gain of 1.

Gain and Offset Adjustments

The SDM853 module has offset and gain adjust potentiometers accessible through two holes on the edge opposite the connector. The RWC-V8/16 card also has two external potentiometers for offset and gain adjustments. The potentiometer located near the edge of the card is for offset adjust.

RWC-V8/16 OPT 001 is supplied with the two Burr-Brown modules installed and the gain and offset correctly adjusted. When installing the Burr-Brown modules on the standard version of RWC-V8/16, the user must adjust the offset and gain using the external and/or internal potentiometers. The test program given in Section 7.7.5 may be used for this purpose, with a standard voltage source.

7.7.4.4 Module Connector Definitions

System Connector

See Section 6.1.4 for the pin definitions.

Device Connector

All the analog input signals are provided via the Device Connector. The 16 input channels are numbered 0 to 15. Pins 1, 19, 20 to 37 are all connected to the SDM853 module analog ground.

Pin definitions for the Device Connector are as follows:

Pin Number	Signal
1	ground
2	not used
3	channel 15
4	channel 7
5	channel 14
6	channel 6
7	channel 13
8	channel 5
9	channel 12
10	channel 4
11	channel 11
12	channel 3
13	channel 10
14	channel 2
15	channel 9
16	channel 1
17	channel 8
18	channel 0
19 to 37	ground

Analog Input Connections

For single-ended inputs, all signal returns must be connected to ground.

For differential inputs, channels 8 to 15 become the signal returns for channels 0 to 7 respectively. The differential input signals must therefore be connected between pin pairs 0-8, 1-9, 2-10,... ....7-15.

Analog Input Requirements

Unused inputs must be connected to ground. When long leads are connected to the inputs, care must be taken to prevent the leads from picking up excessive noise from external equipment and wiring. With low level signals it is advisable to operate in the differential input mode. In this way any noise will be common to both input wires, and rejected due to the high common-mode rejection of the instrumentation amplifier. For best noise rejection, the input wire pairs must be twisted. Shielded twisted pair cables should be used preferably.

The analog inputs are protected from damage by voltages as high as 15.5 volts, and from short spikes of a few microseconds well in excess of this value.

The analog input specifications are as follows:

Max. input voltage without damage	= $\pm$ 16 volts
Max. input voltage for multiplexer operation	= $\pm$ 10.24 volts
Input impedence	= 100 MΩ , 10pF OFF channel 100MΩ , 100pF ON channel

Bias current	
25°C	= 20nA
0°C to 70°C	= 50nA
Differential Bias Current (25°C)	= 10nA
Differential Bias Current Drift	= 0.1nA /°C
Amplifier output noise (Gain = 100, Rs = 500Ω)	= 1.2mV, rms; 7mV, p-p
Amplifier input offset voltage (max)	= 400μV

7.7.4.5 Operational Requirements

Power Requirements

The RWC-V8/16 requires a single +5V power supply from the DCE-BUS. The +15V and -15V supplies for the SDM853 module are generated by the 546 dual power supply module. A typical power requirement in the quiescent state is given below (including the two Burr-Brown modules). Active state value is typically 10% higher.

+5V : 950mA

Environmental Requirements

Operating temperature	: 0°C to 55°C
Storage temperature	: -25°C to +85°C
Relative humidity	: up to 95% noncondensing

Bus Loading

The RWC-V8/16 module presents 1 unit-load to the DCE-BUS (see Section 4.4).

7.7.5 TEST PROCEDURE

This section defines a simple test configuration and a test program for performing a basic functional test on the RWC-V8/16 with the two Burr-Brown modules. Users are advised to carry out such a test procedure when necessary to establish the correct functioning of a module. The test program also provides a good example of RWC-V8/16 module driver software.

Test Configuration

The following test program requires a RWC-V8/16 with the two Burr-Brown modules installed, and a standard voltage source. It tests channel numbers 0 to 9.

```
                        ; THIS IS A SIMPLE PROGRAM FOR TESTING THE STANDARD
                        ; RWC-V8/16 MODULE WITH THE TWO BURR-BROWN MODULES
                        ; INSTALLED & CARD ADDRESS SELECT SWITCH SET TO '1'.
                        ; THE PROGRAM ACCEPTS A CHANNEL NUMBER FROM CONSOLE
                        ; WITH ECHO, AND THEN TYPES OUT THE 12 BIT DIGITAL
                        ; RESULT AS 3 HEX DIGITS, FOLLOWED BY THE CHANNEL
                        ; ADDRESS READ BACK FROM THE SDM853 MODULE. THE
                        ; THE VALUE PRINTED IN RESPONSE TO A CHANNEL ADDRESS
                        ; INPUT FROM CONSOLE WILL GIVE THE RESULT OF THE
                        ; CONVERSION FOR A CHANNEL INPUT TWO STEPS EARLIER.
                        ; AN EXAMPLE OF THE PRINTOUT IS AS FOLLOWS:
                        ;       1 XXXA
                        ;       2 YYY1
                        ;       3 AAA2
                        ;       4 BBB3
                        ;       .
                        ;       .
                        ; 1,2,3,4 ARE CHANNEL ADDRESSES INPUT VIA CONSOLE.
                        ; AAA = RESULT FOR CHANNEL #1,
                        ; BBB = RESULT FOR CHANNEL #2,.....
                        ; THE PROGRAM IS ENTERED FROM THE DCE UTILITY.
                        ;
                        ;
031E                    RDRWC   EQU     031EH
0349                    WRRWC   EQU     0349H
061F                    TCRLF   EQU     061FH
053A                    TSP     EQU     053AH
05FD                    TADDR   EQU     05FDH
0561                    CIE     EQU     0561H
```

```
1000                    ORG     1000H
                                ;
                                ; INITIALIZATION
1000 3E13       INIT:   MVI     A,13H
               +        STGI    1       ; SELECT RIC COMMAND REGISTER
1002 32011C
1005 3EB0               MVI     A,0B0H
1007 CD4903             CALL    WRRWC   ; CONFIGURE RIC PORTS
100A 3E11               MVI     A,11H
               +        STGI    1       ; SELECT RIC PORT 1
100C 32011C
100F AF                 XRA     A
1010 CD4903             CALL    WRRWC   ; ENABLE RESET (DISABLED LATER)
                                ;
1013 3E11       LOOP:   MVI     A,11H
               +        STGI    1       ; SELECT RIC PORT 1
1015 32011C
1018 CD1F06             CALL    TCRLF   ; NEW LINE
101B CD6105             CALL    CIE     ; WAIT FOR CONSOLE INPUT & ECHO
101E 47                 MOV     B,A     ; SAVE
101F CD3A05             CALL    TSP     ; TYPE SPACE
1022 78                 MOV     A,B     ; RESTORE DATA
1023 E60F               ANI     0FH     ; IGNORE 4 UPPER BITS
1025 F6A0               ORI     0A0H    ; INSERT CONTROL CHARACTERS FOR
                                ;    RANDOM ADDRESSING.
1027 CD4903             CALL    WRRWC   ; WRITE TO RIC PORT 1
102A 3E10               MVI     A,10H
               +        STGI    1       ; SELECT RIC PORT 0
102C 32011C
102F CD1E03             CALL    RDRWC   ; READ LOW ORDER 4 BITS OF RESULT
                                ;    AND LATCHED CHANNEL ADDRESS,
                                ;    TRIGGER CONVERSION OF LATCHED
                                ;    ADDRESSED CHANNEL, AND
                                ;    LATCH NEW ADDRESS FROM RIC
                                ;    PORT 1 BITS 0-3.
1032 6F                 MOV     L,A     ; STORE
1033 CD1E03             CALL    RDRWC   ; READ HIGH ORDER 8 BITS OF RESULT
1036 67                 MOV     H,A
1037 CDFD05             CALL    TADDR   ; PRINT THE RESULT AS 3 HEX DIGITS
                                ;    FOLLOWED BY ADDRESS OF CHANNEL
                                ;    FOR NEXT CONVERSION.
103A C31310             JMP     LOOP    ; CONTINUE
0000                    END
```

7.7.6 ORDERING INFORMATION

RWC-V8/16 : Standard Version, supplied without the two Burr-Brown modules.

RWC-V8/16M : Standard Version with the Burr-Brown modules SDM853 and 546 installed and tested.

7.8 RWC-IEC : IEC INSTRUMENTATION BUS INTERFACE

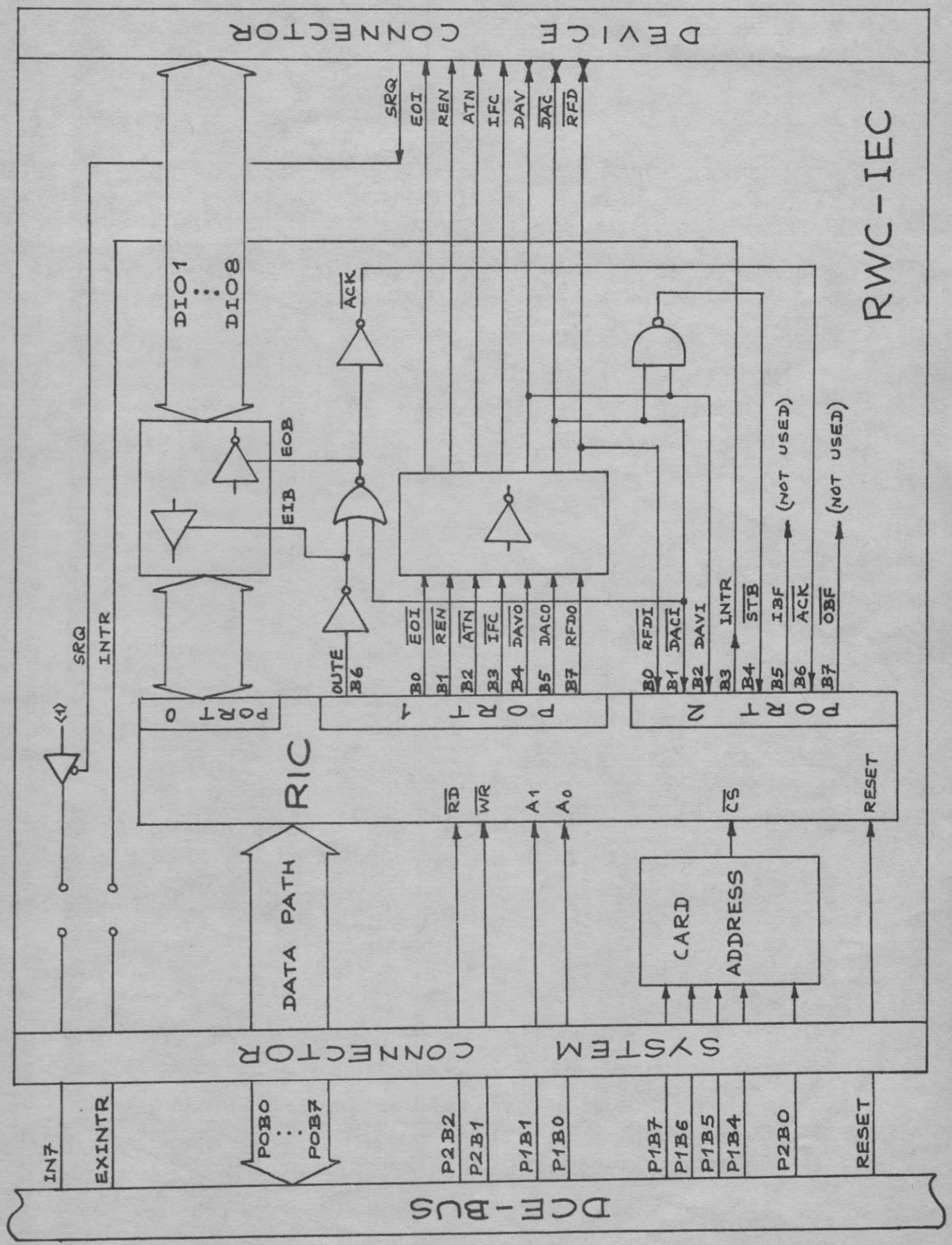
7.8.1 FUNCTIONAL DESCRIPTION

The RWC-IEC Real-World interface module allows the DCE processor to control IEC bus compatible instruments, conforming to International Electrotechnical Commission recommendations. It provides a link between the DCE-BUS and the IEC-BUS by allowing the DCE microcomputer to act as an IEC-BUS controller. It enables DCE control of a cluster of IEC/IEEE Bus compatible instruments supplied by Hewlett-Packard, Fluke, Tektronix, Wavetek, Rohde & Schwarz etc. Each card has an identification address defined by a hexadecimal switch and up to fifteen cards may be directly connected to the DCE-BUS.

7.8.2 FEATURES

- enables DCE microcomputer control of IEC-BUS.
- software driven Control, Source and Accepter functions.
- IEC Service Request processable via DCE interrupt.
- standard IEC connector installed on module.
- standard hardware and software interface to DCE-BUS.
- selectable card address.
- single 100 x 160 mm eurocard format.

7.8.3 FUNCTIONAL BLOCK DIAGRAM



7.8.4 SYSTEM DESIGN PARAMETERS

7.8.4.1 Hardware Configuration

The functional block diagram in Section 7.8.3 illustrates the hardware configuration of the RWC-IEC module.

The eight DIO signal lines for carrying interface messages to and from the IEC-BUS are provided via Port 0 operating in bi-directional mode. The output signals are buffered via 7438 devices performing as inverters.

The three interface signal lines DAV, $\overline{\text{RFD}}$, $\overline{\text{DAC}}$ used to effect the transfer of each byte of data on the DIO signal lines, are output via Port 1 Bits 4,7,5 and input via Port 2 Bits 2,0,1 respectively. Handshake control signals necessary for maintaining proper Port 0 bus flow discipline are generated on the module.

The device Service Request (SRQ) and the RIC Interrupt Request are jumper connectable to DCE-BUS interrupt request lines IN7 and EXINTR.

7.8.4.2 Programming Specifications

The RWC-IEC module is addressed via the standard DCE-BUS interface. Programming specifications for driving the DCE-BUS are given in Section 4.1.

RIC Initialization

The RIC on the RWC-IEC module should be initialized by writing the control word C1H to the RIC Command Register. This configures Port 0 as bi-directional, Port 1 as output and Port 2 Bits 0,1,2 as input. Port 2 Bits 3-7 provide the "Handshaking" signals necessary to maintain proper bus flow discipline.

RIC Device Addresses

The RIC on the RWC-IEC module has three data ports and a command register. Different modes of communication between RIC Ports 0, 1, 2 and the DCE-BUS Data Path are established depending on the Device Address received by the RWC-IEC module from the DCE-BUS. The following table shows the Device Addresses needed for different communication modes:

DEVICE ADDRESS (HEX)	$\overline{RD}$	$\overline{WR}$	OPERATION
Y0	0	1	RIC Port 0 → DCE Data Bus
Y1	0	1	Invalid Operation
Y2	0	1	RIC Port 2 → DCE Data Bus
Y3	0	1	Illegal Condition
Y0	1	0	DCE Data Bus → RIC Port 0
Y1	1	0	DCE Data Bus → RIC Port 1
Y2	1	0	Invalid Operation
Y3	1	0	DCE Data Bus → RIC Command Register
ZX	X	X	RIC Data Bus in 3-state

Notes:

1. Y is the card address select switch setting in hex (1 to F).
2. Z is any number other than Y.
3. X means don't care.
4. Bit numbers 2 and 3 in the Device Addresses are don't care states.
5. RDRWC and WRRWC software routines provide the $\overline{RD}$ and $\overline{WR}$ signals accordingly.

Table 7.8.1 : Device Address Table for RWC-IEC

Format and Interpretation of Data

For full details of the electrical realization of the IEC-BUS interface refer to Section 3 of the publication "Standard Interface Systems for Programmable measuring Apparatus" by the International Electrotechnical Commission (IEC). Note that all active low signals indicated by a preceding 'N' in the above publication are shown in this manual with a bar (eg. NDAC appears as $\overline{\text{DAC}}$). A brief summary of the IEC-BUS interface signals is given below.

The IEC-BUS structure is organized into three sets of signal lines:

- data bus (8 lines)
- data byte transfer control bus (3 lines)
- general interface management bus (5 lines)

a) Data Bus

A set of eight interface signal lines carries all 7-bit interface messages and the device dependent messages:

DATA INPUT-OUTPUT 1 (DIO1)
:
DATA INPUT-OUTPUT 8 (DIO8)

Message bytes are carried on the DIO signal lines:

- in a bit-parallel/byte-serial form;
- asynchronously;
- bi-directionally.

Note: A message may be carried on an individual DIO signal line when required.

b) Data Byte Transfer Control Bus

A set of three interface signal lines is used to effect the transfer of each byte of data on the DIO signal lines from an addresses talker to all addressed listeners:

- DATA VALID (DAV) is used to indicate the condition (availability and validity) of information on the DIO signal lines.

- READY FOR DATA ($\overline{\text{RFD}}$) is used to indicate the condition of readiness of device(s) to accept data.

- DATA ACCEPTED ($\overline{\text{DAC}}$) is used to indicate the condition of acceptance of data by device(s).

The DAV, $\overline{\text{RFD}}$ and $\overline{\text{DAC}}$ signal lines operate in what is called a three-wire (interlocked) handshake process to transfer each data byte across the interface.

c) General Interface Management Bus

- ATTENTION (ATN) is used to specify how data on the DIO signal lines are to be interpreted and which devices must respond to the data.

- INTERFACE CLEAR (IFC) is used to place the interface system, portions of which are contained in all interconnected devices, in a known quiescent state.

- SERVICE REQUEST (SRQ) is used by a device to indicate the need for attention and to request an interruption of the current sequence of events.

- REMOTE ENABLE (REN) is used (in conjunction with other messages) to select between two alternate sources of device programming data.

- END OR IDENTIFY (EOI) is used to indicate the end of a multiple byte transfer sequence or, in conjunction with ATN, to execute a parallel polling sequence.

Signal allocation for the RIC port bits are as follows:

Port 0 :	b0 - b7	=	DIO1 - DIO8	
Port 1 :	b0	=	$\overline{\text{EOI}}$	(EOI - output)
	b1	=	$\overline{\text{REN}}$	(REN - output)
	b2	=	$\overline{\text{ATN}}$	(ATN - output)
	b3	=	$\overline{\text{IFC}}$	(IFC - output)
	b4	=	$\overline{\text{DAVO}}$	(DAV - output)
	b5	=	DACO	($\overline{\text{DAC}}$ - output)
	b7	=	RFDO	($\overline{\text{RFD}}$ - output)
	b6	=	OUTE	(input/output bus control)
Port 2 :	b0	=	$\overline{\text{RFDI}}$	($\overline{\text{RFD}}$ - input)
	b1	=	$\overline{\text{DACI}}$	($\overline{\text{DAC}}$ - input)
	b2	=	DAVI	(DAV - input)
	b3	=	INTR	
	b4	=	$\overline{\text{STB}}$	
	b5	=	IBF	
	b6	=	$\overline{\text{ACK}}$	
	b7	=	$\overline{\text{OBF}}$	

Special Considerations

Input signals $\overline{\text{RFDI}}$, $\overline{\text{DACI}}$, DAVI available at Port 2 Bits 0, 1, 2 are used for indicating the IEC-BUS status to the DCE controller.

Handshake control signals $\overline{\text{ACK}}$ and $\overline{\text{STB}}$ are generated automatically when data is transferred to and from the IEC-BUS.

Signals EIB and EOB which enable the input and output buffers are derived from the DCE output signal OUTE and the IEC-BUS input signal $\overline{\text{DACI}}$. OUTE must be controlled by the DCE processor accordingly.

7.8.4.3 User Options

Interrupt Generation Jumpers

A jumper network allows the user to connect the Service Request signal SRQ from the IEC-BUS and the RIC interrupt request signal INTR, to interrupt lines IN7 and EXINTR on the DCE-BUS.

7.8.4.4 Module Connector Definitions

System Connector

See Section 6.1.4 for the pin definitions.

Device Connector

This is the special IEC Bus Compatible 24 pin female connector, capable of accepting the locking screws of the cable assembly.

Contact definition is as follows:

Contact No.	Signal Line
1	DIO1
2	DIO2
3	DIO3
4	DIO4
5	EOI
6	DAV
7	NRFD
8	NDAC
9	IFC
10	SRQ
11	ATN
12	SHIELD

Contact No.	Signal Line
13	DIO5
14	DIO6
15	DIO7
16	DIO8
17	REN
18	Gnd, (6)
19	Gnd, (7)
20	Gnd, (8)
21	Gnd, (9)
22	Gnd, (10)
23	Gnd, (11)
24	Gnd, LOGIC

Note: Gnd (n) refers to the signal ground return of the referenced contact.

7.8.4.5 Operational Requirements

Signal Characteristics

All the output signals are buffered via 7438 devices performing as inverters.

Power Requirements

The RWC-IEC card uses a single +5 volt supply. Typical power consumption is:

+5 V : 150mA

Environmental Requirements

Operating temperature	:	0°C to 55°C
Storage temperature	:	-25°C to +85°C
Relative humidity	:	95% noncondensing

Bus Loading

The RWC-IEC module presents 1 unit-load to the DCE-BUS (see Section 4.4).

7. 8. 6 ORDERING INFORMATION

RWC-IEC : Standard Version