## 7.5 RWC-MI : MATRIX INTERFACE

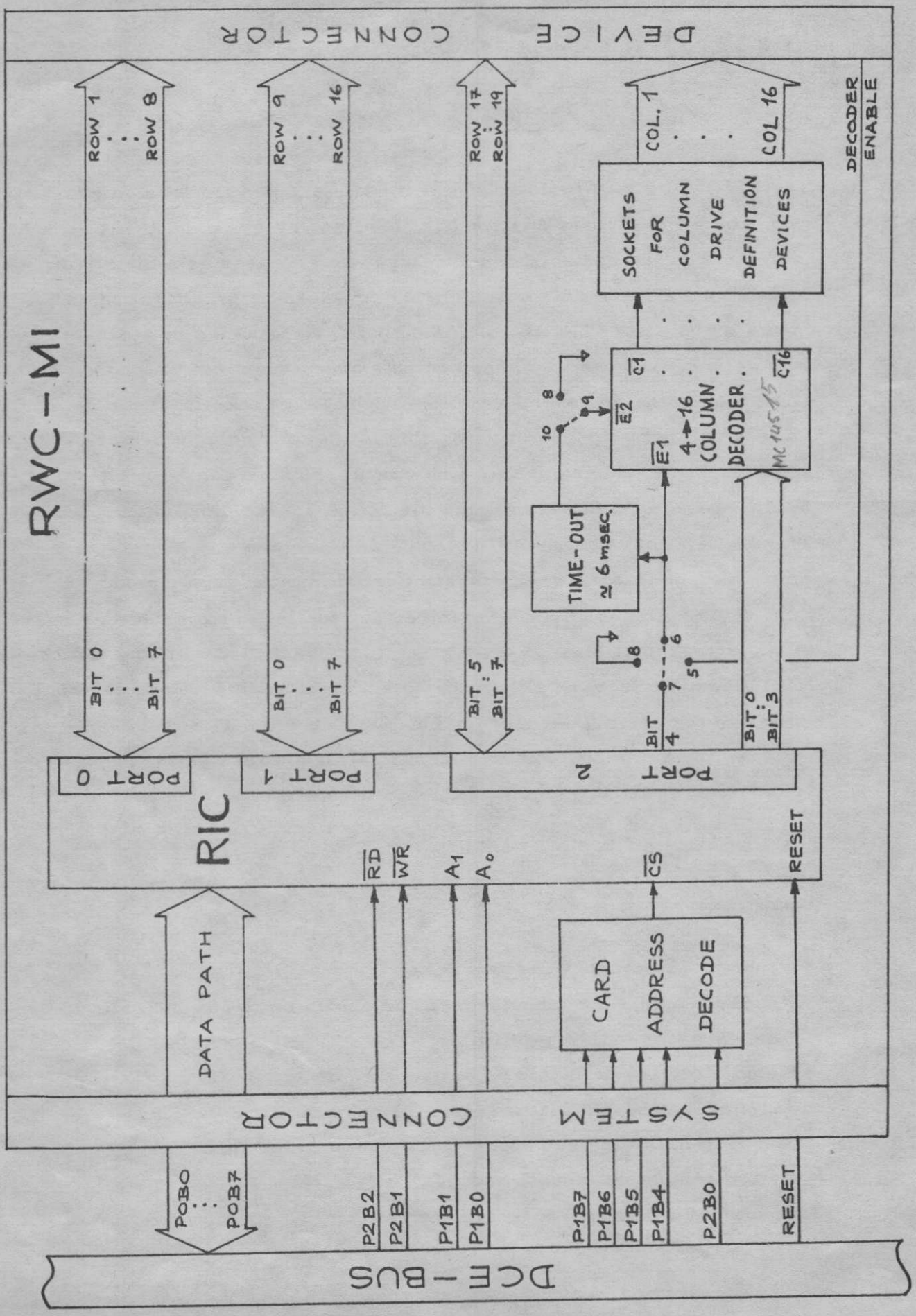
### 7.5.1 FUNCTIONAL DESCRIPTION

The RWC-MI Real-World interface module enables the DCE microcomputer to read up to 304 contact closures, or drive up to 304 indicators. The contacts or indicators are accessed as a matrix of up to 19 rows by 16 columns. The 19 rows can be programmed as inputs or outputs. The 16 column outputs are provided by a decoder with active-low outputs. These outputs are brought out to the device connector at the end of the module through four sockets. Four 2-input NAND gate devices are installed in the four column driver sockets, for producing active-high outputs. These can be replaced by AND gates or connecting links for active-low column outputs. The RWC-MI module has a 'time-out' safety feature to protect LED or similar indicators when operating in the matrix driver mode. If this feature is enabled via the jumper option, the column decoder has to be refreshed at least every 5 msec to prevent it from being turned-off. A jumper network allows the selection of an internal or external signal as the column decoder enable, with or without the time-out feature. Each module has an identification address defined by a hexadecimal switch, and upto fifteen can be directly connected to the DCE-BUS.

### 7.5.2 FEATURES

- 19 row x 16 column matrix access.
- Reads up to 304 contact closures, or drives up to 304 indicators.
- Rows programmable as input or output.
- Column outputs definable as active-high or active-low.
- Automatic time-out feature for LED protection.
- Standard hardware and software interface to the DCE-BUS.
- Switch selectable module address.
- Single 100 x 160 mm eurocard format.

## 7.5.3 FUNCTIONAL BLOCK DIAGRAM



## 7.5.4 SYSTEM DESIGN PARAMETERS

### 7.5.4.1 Hardware Configuration

The functional block diagram in Section 7.5.3 illustrates the hardware configuration of the RWC-MI module. The column decoder provides 16 active-low outputs, which may be converted to active-high if necessary. The column time-out feature is implemented by a monostable.

The RWC-MI module is supplied with quadruple 2-input NAND gates (7400) already installed in the four column driver sockets. One of the inputs to each gate is connected to logic 1 on the module, for converting the column decoder outputs to active-high. If active-low column outputs are desired, these four quadruple gates can be replaced by pin-compatible AND gates or connecting links.

Jumper networks 5-6-7-8 and 8-9-10 allow the selection of an internal or external signal as the column decoder enable, with or without the time-out feature. The module is supplied with jumpers 6-7 and 9-10 already installed to select RIC Port 2 Bit 4 as the column decoder enable, with the time-out feature.

When the column decoder is disabled (ie one or both of $\overline{E1}$ and $\overline{E2}$ are low), all 16 outputs will be high irrespective of the value of the 4 inputs.

### 7.5.4.2 Programming Specifications

The RWC-MI module is addressed via the standard DCE-BUS interface. Programming specifications for driving the DCE-BUS are given in Section 4.1.

RIC Configuration

The RIC on the RWC-MI module can be configured for row input or row output. The 4 binary coded column lines must always be configured in the output mode.

When the RWC-MI module is used as a normal matrix driver, the rows must be configured in the output mode by writing control word 80H to the RIC Command Register. This will configure all 3 RIC ports in output mode.

When the RWC-MI module is used in normal matrix read applications, the rows must be configured in the input mode by writing control word 9AH to the RIC Command Register. This will configure RIC Port 0, Port 1 and Bits 4-7 of Port 2 in the input mode, while the column bits 0-3 of Port 2 remain in the output mode.

RIC Device Addresses

The RIC on the RWC-MI module has 3 data ports and a command register. Different modes of communication between RIC Ports 0,1,2 and the DCE-BUS Data Path are established, depending on the Device Address received by the RWC-MI module from the DCE-BUS. The following table shows the Device Addresses needed for different communication modes.

| DEVICE ADDRESS (HEX) | $\overline{RD}$ | $\overline{WR}$ | OPERATION |
|---|---|---|---|
| Y0 | 0 | 1 | RIC Port 0 → DCE Data Bus |
| Y1 | 0 | 1 | RIC Port 1 → DCE Data Bus |
| Y2 | 0 | 1 | RIC Port 2 → DCE Data Bus |
| Y3 | 0 | 1 | Illegal Condition |
| Y0 | 1 | 0 | DCE Data Bus → RIC Port 0 |
| Y1 | 1 | 0 | DCE Data Bus → RIC Port 1 |
| Y2 | 1 | 0 | DCE Data Bus → RIC Port 2 |
| Y3 | 1 | 0 | DCE Data Bus → RIC Command Register |
| ZX | X | X | RIC Data Bus in 3-state |

Notes:

1. Y is the card address select switch setting in hex (1 to F).
2. Z is any number other than Y.
3. X means don't care.
4. Bits 2 and 3 in the Device Addresses are don't care states.
5. RDRWC and WRRWC software routines provide the $\overline{RD}$ and $\overline{WR}$ signals accordingly.

Table 7.5.1 : Device Address Table for RWC-MI

Format of Data

RIC Port 2 Bits 0-3 are decoded by the 4 to 16 decoder to provide the 16 column outputs. Port 2 Bit 4 can be used either as the decoder enable signal (output), or as a status indicator (input). This bit must be configured together with Port 2 Bits 5-7.

RIC Port bit usage is summarized below:

| | | | |
|---|---|---|---|
| Port 0 : | b0 - b7 | = | rows 1 to 8, as input or output |
| Port 1 : | b0 - b7 | = | rows 9 to 16, as input or output |
| Port 2 : | b5 - b7 | = | rows 17 to 19, as input or output |
| | b4 | = | status indicator input, or column decoder enable output |
| | b0 - b3 | = | binary coded column select outputs. |

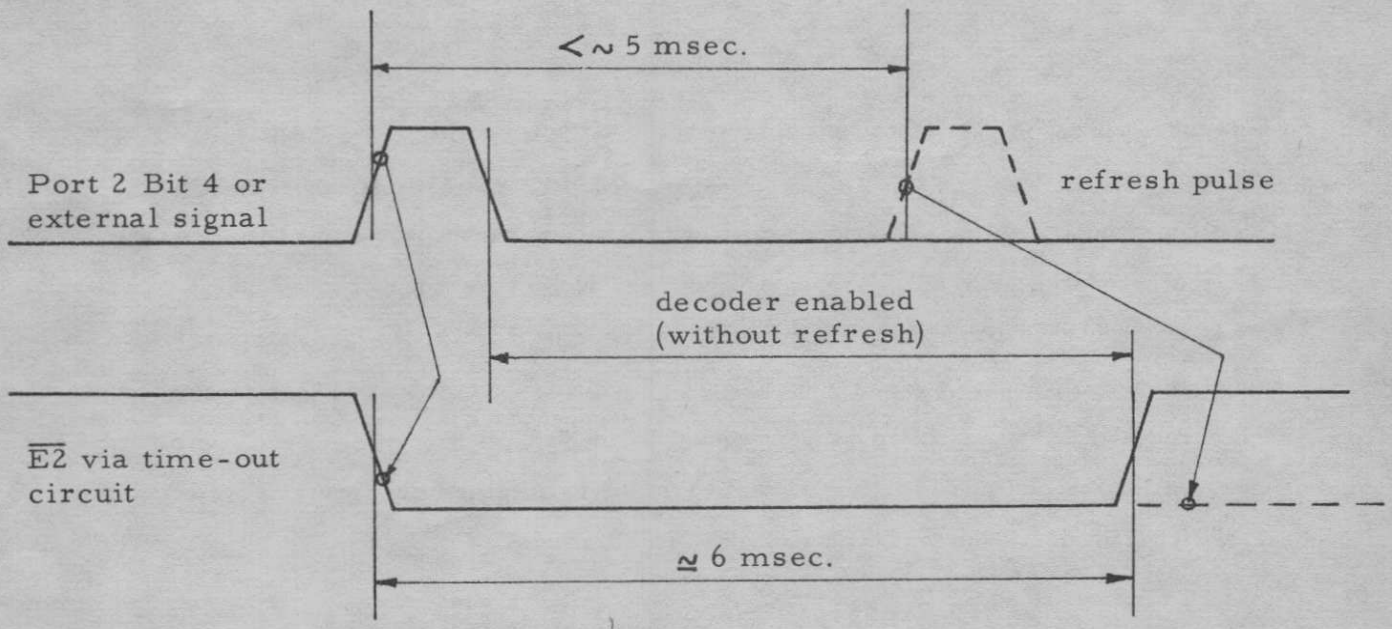
Interpretation of Data

The 4 binary coded column select bits output from Port 2 Bits 0-3 are decoded by the 4 to 16 decoder with inverting outputs, to select one of the 16 columns. The actual polarity of the column outputs from the RWC-MI module will depend on the column driver devices selected. All zeroes at Port 2 Bits 0-3 will select column 1 (device connector pin 1); all ones will select column 16 (device connector pin 16).

Special Considerations

When rows 17 to 19 are configured in the input mode, Port 2 Bit 4 will also function in input mode. Therefore it cannot be used for providing the decoder enable signal. In such a configuration the decoder must be permanently enabled by connecting jumpers 6-8 and 8-9, or activated by an external enable signal (device connector pin 17) with jumpers 5-6 and 8-9 or 9-10 connected.

The RWC-MI module has a 'time-out' safety feature to protect LED or similar indicators when operating in the matrix driver mode. If this feature is enabled via the jumper option, the column decoder has to be refreshed at least every 5 msec to prevent it from being turned off. This is achieved by pulsing Port 2 Bit 4 or the external column enable signal, at regular time intervals not greater than about 5 msec. The diagram below shows the sequence of operation:




When Port 2 Bit 4 is configured in the input mode and the external column enable signal is selected, it is possible to use the latter signal as a data ready indicator by connecting jumpers 5-6-7, and software scanning Port 2 Bit 4.

If the column decoder is permanently enabled by jumpers across 6-8 and 8-9, it is possible to use Port 2 Bit 4 as an extra row by a jumper across 5-7. In this case, Port 2 Bits 4-7 can be software configured as rows 17-20. Row 20 will then be available at device connector pin 17.

## RWC-MI RIC / DCE-BUS Protocol

### Initialization

The RWC-MI module RIC should first be initialized by writing a suitable control word to its Command Register. The only constraint here is that Port 2 Bits 0-3 must be in output mode. All the other RIC Port bits may be configured as input, output or a combination of both. Normally, the rows are all configured as input by writing control word 80H, or as output by writing control word 9AH to the RIC Command Register.

### Matrix Read Operation

Configure the RIC Ports as required. Select the required column by sending the corresponding binary value to the column decoder via Port 2 Bits 0-3. If the decoder is not permanently enabled, enable it either via Port 2 Bit 4 or an external enable signal. If Port 2 Bits 4-7 are configured in input mode, the decoder enable signal cannot come from Port 2 Bit 4. For matrix read operations the time-out feature is normally de-selected, and the decoder may be permanently enabled if desired. Now read the row inputs from Port 0, Port 1 and Bits 5-7 of Port 2, in any order.

### Matrix Drive Function

Configure the RIC ports as required. Select the required column via Port 2 Bits 0-3 as before. For matrix driving, the decoder enable signal is normally obtained from Port 2 Bit 4, or an external source. If the time-out feature is selected, this enable signal should be pulsed regularly at time intervals not greater than about 5 msec. Select the required rows by suitable output to Port 0, Port 1 and bits 5-7 of Port 2.

When changing the column decoder and row outputs, transient spurious activations of matrix indicator elements may take place. This is because several program steps are needed to achieve a change-over

from one matrix element activation to another. Such spurious activations may be eliminated if necessary by keeping the decoder disabled while the new row and column values are set up.

See Section 7.5.5 for a Programming example.

### 7.5.4.3 User Options

#### Column Drivers

The 4 to 16 column decoder provides 16 active-low outputs. These outputs are channeled via four sockets on the module. By the insertion of suitable gates into these sockets, the column outputs from the RWC-MI module may be configured as active-high or active-low.

The module is supplied with four 7400 NAND gates already installed in the sockets, to provide active-high column outputs.

If active-low column outputs are desired, replace these devices with four pin-compatible AND gates (7408 or 7409), or component carriers with links across pins 2-3, 5-6, 9-8 and 12-11.

#### Column Decoder Enable and Time-Out Jumpers

The column decoder has two active low enable signals $\overline{E1}$, $\overline{E2}$. Jumper network 5-6-7-8 allows $\overline{E1}$ to be connected to Port 2 Bit 4 (link 6-7), the external enable signal via device connector pin 17 (link 5-6), or grounded for permanent enable (link 6-8).

Enable signal $\overline{E2}$ may be grounded for permanent enable (link 8-9), or derived via the time-out circuit (link 9-10).

Note: When Port 2 Bit 4 is configured in the input mode and the external column enable signal is utilized, it is possible to use the latter signal as a data ready indicator by connecting jumpers 5-6-7 and scanning Port 2 Bit 4.

### 7.5.4.4 Module Connector Definitions

System Connector

See Section 6.1.4 for the pin definitions.

Device Connector

| Pin Number | Signal | Input/Output |
|---|---|---|
| 1 | Column 1 | O/P |
| 2 | " 2 | " |
| 3 | " 3 | " |
| 4 | " 4 | " |
| 5 | " 5 | " |
| 6 | " 6 | " |
| 7 | " 7 | " |
| 8 | " 8 | " |
| 9 | " 9 | " |
| 10 | " 10 | " |
| 11 | " 11 | " |
| 12 | " 12 | " |
| 13 | " 13 | " |
| 14 | " 14 | " |
| 15 | " 15 | " |
| 16 | " 16 | " |
| 17 | Column decoder enable | I/P |
| 18 | Row 18 (Port 2 Bit 6) | I/O |
| 19 | Ground | - |
| 20 | Row 9 (Port 1 Bit 0) | I/O |
| 21 | Row 10 (Port 1 Bit 1) | " |
| 22 | Row 11 (Port 1 Bit 2) | " |
| 23 | Row 12 (Port 1 Bit 3) | " |
| 24 | Row 13 (Port 1 Bit 4) | " |
| 25 | Row 14 (Port 1 Bit 5) | " |
| 26 | Row 15 (Port 1 Bit 6) | " |
| 27 | Row 16 (Port 1 Bit 7) | " |
| 28 | Row 8 (Port 0 Bit 7) | " |
| 29 | Row 7 (Port 0 Bit 6) | " |
| 30 | Row 6 (Port 0 Bit 5) | " |
| 31 | Row 5 (Port 0 Bit 4) | " |
| 32 | Row 4 (Port 0 Bit 3) | " |
| 33 | Row 3 (Port 0 Bit 2) | " |
| 34 | Row 2 (Port 0 Bit 1) | " |
| 35 | Row 1 (Port 0 Bit 0) | " |
| 36 | Row 19 (Port 2 Bit 7) | " |
| 37 | Row 17 (Port 2 Bit 5) | " |

Note: the row and column numbering is arbitary.

### 7.5.4.5 Operational Requirements

#### Signal Characteristics

All the row output lines are capable of driving one standard TTL load. They can drive a Darlington configuration (1.5V) and source up to 1mA.

The column decoder has active low outputs and can drive up to 10 standard TTL loads. The actual characteristics of column output signals available at the device connector depend on the column driver devices inserted by the user.

#### Power Requirements

The RWC-MI card uses a single +5 volt supply. Typical power consumption is:

+5V : 150mA

#### Environmental Requirements

| | | |
|---|---|---|
| Operating temperature | : | 0°C to 55°C |
| Storage temperature | : | -25°C to +85°C |
| Relative humidity | : | 95% noncondensing |

#### Bus Loading

RWC-MI module presents 1 unit-load to the DCE-BUS (see Section 4.4 ).

### 7.5.5 TEST PROCEDURE

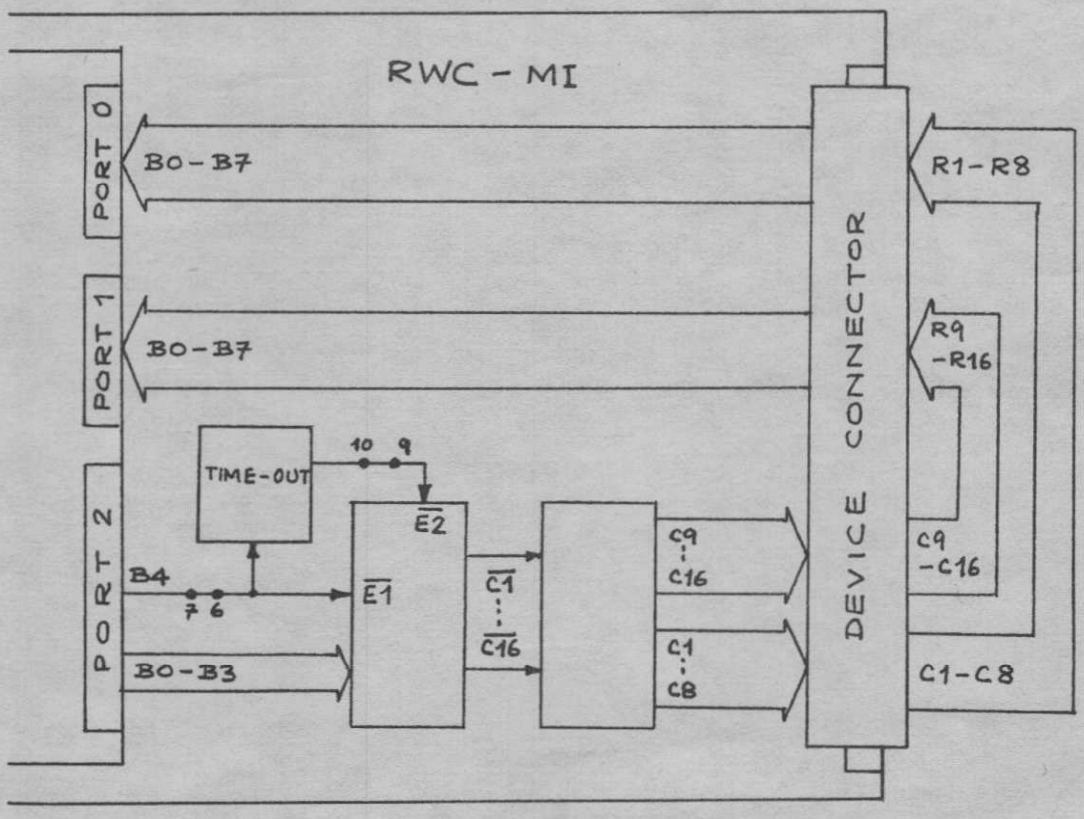
This section defines a simple test configuration and a test program for performing a basic functional test on the RWC-MI module. Users are advised to carry out such a test procedure when necessary to

establish the correct functioning of a module. The test program also provides a good example of RWC-MI module driver software.

Test Configuration

The following test program relates to the test configuration below. It requires a standard RWC-MI module with active-high column outputs, jumpers 6-7,9-10 connected, and a simple test harness at the device connector to feed the column outputs back as 16 row inputs. Columns 1 to 8 are fed into Port 0 Bits 0-7, and columns 9 to 16 are fed into Port 1 Bits 0-7. See Section 7.5.4.4 for corresponding device connector pin definitions. The RWC-MI RIC is configured with Port 0, Port 1 in the input mode, and Port 2 in the output mode.

This scheme does not test rows 17-19 (Port 2 Bits 5-7).



RWC-MI Test Program

```
0000                ; THIS IS A SIMPLE PROGRAM FOR TESTING THE STANDARD
0000                ; RWC-MI MODULE WITH CARD ADDRESS SELECT SWITCH = 'A',
0000                ; ACTIVE-HIGH COLUMN OUTPUTS AND JUMPERS 6-7, 8-9.
0000                ; THE COLUMN OUTPUTS ARE FED BACK AS 16 ROW INPUTS.
0000                ; ALL THE 16 COLUMNS ARE SELECTED IN SEQUENCE AND
0000                ; VERIFIED AGAINST THE INPUT READ FROM PORTS 0 AND 1.
0000                ; FOR EVERY MISMATCH, THE CODED 4-BIT COLUMN VALUE
0000                ; IS PRINTED ON CONSOLE AS A HEX DIGIT PRECEDED BY 0,
0000                ; FOLLOWED BY READING FROM PORT 1 AND 0 AS 4 HEX
0000                ; DIGITS (16 ROW INPUTS).
0000                ; PROGRAM IS ENTERED FROM UTILITY AND RETURNS TO THE
0000                ; UTILITY AT THE END. DCE-DM WITH RESIDENT ASSEMBLER
0000                ; AND DCE-2 VERSION 2.0 UTILITY HAS BEEN USED.
0000                ;
02EC                CMPDB:  EQU     02EC
031E                RDRWC:  EQU     031E
0349                WRRWC:  EQU     0349
061F                TCRLF:  EQU     061F
0602                TBYTE:  EQU     0602
053A                TSP:    EQU     053A
05FD                TADDR:  EQU     05FD
0000                ;
1000                        ORG     1000
1000 3EA3           INIT:   MVI     A,0A3   ; CONFIGURE RIC PORTS 0,1 AS
1002 32011C                 STGI    1       ;    INPUT; 2 AS OUTPUT.
1005 3E92                   MVI     A,92
1007 CD4903                 CALL    WRRWC
100A 0600                   MVI     B,00    ; B CONTAINS COPY OF OUTPUT
100C                                        ;    TO RIC PORT 2.
100C 210100                 LXI     H,1     ; H,L CONTAINS CORRECT ROW
100F                                        ;    VALUE EXPECTED.
100F CD2410         LOOP:   CALL    NEWCL   ; REFRESH COLUMN DECODER AND
1012                                        ;    WRITE NEW COLUMN VALUE.
1012 CD3710                 CALL    RDROW   ; READ ROW INPUT INTO D,E
1015 CDEC02                 CALL    CMPDB   ; COMPARE H,L AND D,E
1018 C44A10                 CNZ     ERR     ; IF UNEQUAL PRINT DATA
101B 3E0F                   MVI     A,0F
101D B8                     CMP     B       ; TEST FOR END
101E C8                     RZ              ; IF SO RETURN TO UTILITY
101F 04                     INR     B       ; NEXT COLUMN OUTPUT
1020 29                     DAD     H       ; NEW ROW VALUE EXPECTED
1021 C30F10                 JMP     LOOP    ; CONTINUE TILL END
1024                                        ;
1024                        ; THIS ROUTINE OUTPUTS A NEW COLUMN VALUE AND
1024                        ;      REFRESHES DECODER BY PULSING BIT 4.
1024                        ;
1024 3EA2           NEWCL:  MVI     A,0A2
1026 32011C                 STGI    1       ; SELECT RIC PORT 2
1029 78                     MOV     A,B     ; BIT 4 = 0 BITS 0-3=COLUMNS
102A CD4903                 CALL    WRRWC
102D F610                   ORI     10
102F CD4903                 CALL    WRRWC   ; BIT 4=1 REST SAME
1032 78                     MOV     A,B     ; BIT 4=0
1033 CD4903                 CALL    WRRWC
1036 C9                     RET
```

```
1037                    ; THIS ROUTINE READS PORT 0 INTO E AND PORT 1
1037                    ;       INTO D, AS THE 16 ROW INPUTS.
1037                    ;
1037 3EA0       RDROW:  MVI     A,0A0
1039 32011C             STGI    1       ; SELECT RIC PORT 0
103C CD1E03             CALL    RDRWC   ; READ INTO A
103F 5F                 MOV     E,A     ; STORE
1040 3EA1               MVI     A,0A1
1042 32011C             STGI    1       ; SELECT RIC PORT 1
1045 CD1E03             CALL    RDRWC   ; READ INTO A
1048 57                 MOV     D,A     ; STORE
1049 C9                 RET
104A                                    ;
104A                    ; ERROR PRINT ROUTINE TO PRINT COLUMN CODE
104A                    ;     AS A HEX DIGIT PRECEDED BY A SPACE,
104A                    ;     FOLLOWED BY READ ROW VALUE AS 4 HEX
104A                    ;     DIGITS (ONLY ONE BIT MUST BE SET IN THESE
104A                    ;     16 ROW BITS).
104A                    ;
104A CD1F06     ERR:    CALL    TCRLF   ; NEW LINE
104D 78                 MOV     A,B
104E CD0206             CALL    TBYTE   ; PRINT COLUMN VALUE
1051 CD3A05             CALL    TSP     ; PRINT SPACE
1054 EB                 XCHG            ; MOVE D,E TO H,L
1055 CDFD05             CALL    TADDR   ; PRINT H,L
1058 EB                 XCHG            ; RESTORE
1059 C9                 RET
                        END
```

## 7.5.6 ORDERING INFORMATION

RWC-MI : Standard Version including four 7400 quadruple NAND gates for column driving.

## 7.6 RWC-AI : QUAD-SLOPE ANALOG INPUT MODULES

### 7.6.1 FUNCTIONAL DESCRIPTION

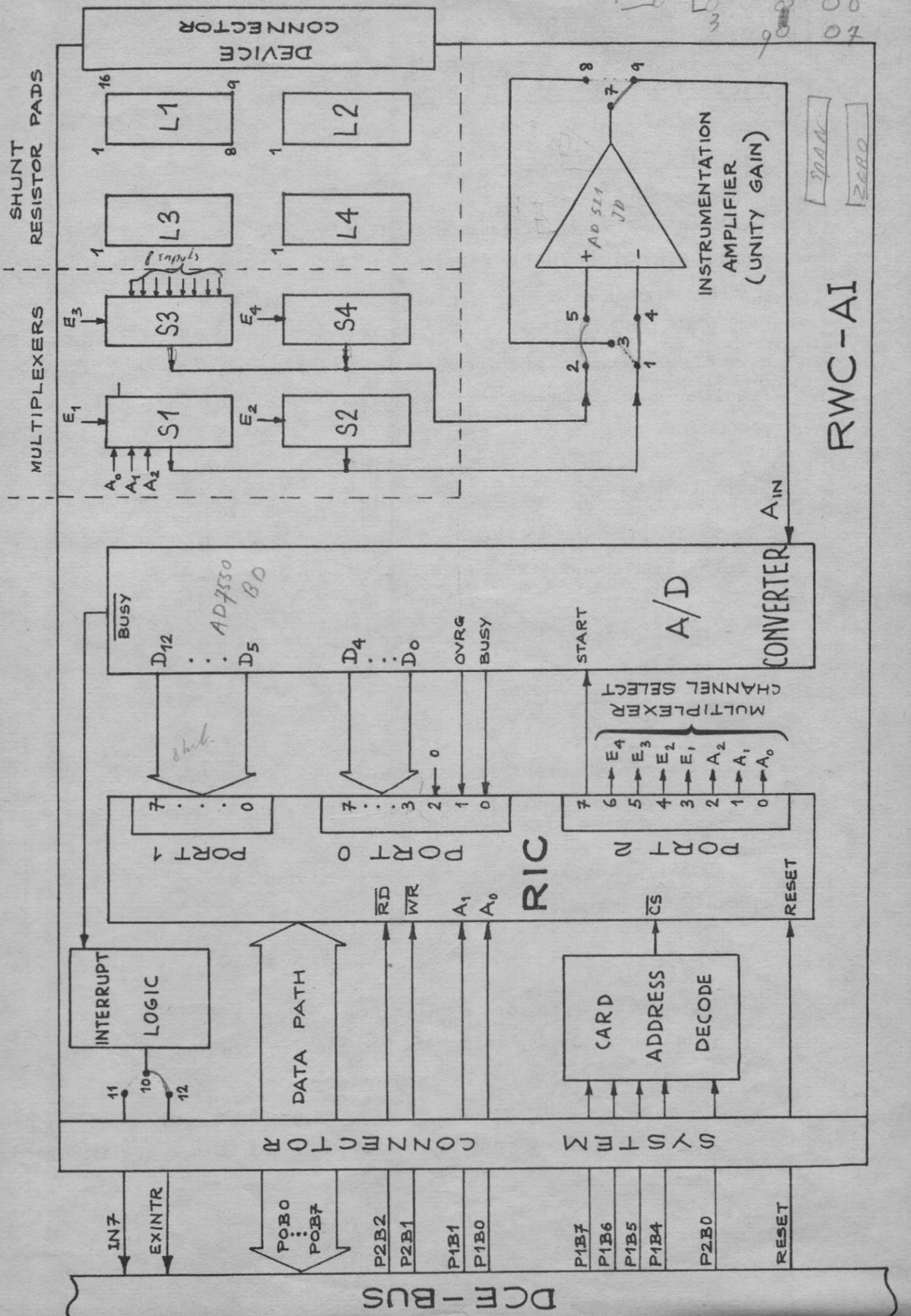
The RWC-AI Real-World interface modules economically enable the input and conversion of multiple analog voltages or currents to digital values suitable for input to a DCE processor module.

Different card configurations provide channel selection and A/D conversion capability for up to 32 single-ended or 16 differential voltage or current input signals. Digital outputs are 13 bits including sign, with 10 or 13 bit resolution. The quad-slope A/D converter provides maximum signal noise rejection with a 80mS conversion time. A jumper choice enables the generation of an interrupt via the DCE-BUS at the end of the conversion. Each card has an identification address defined by a hexadecimal switch, and up to 15 cards may be directly connected to the DCE-BUS.

### 7.6.2 FEATURES

- low-cost configurations for 16 or 32 single-ended voltage inputs, ± 2.5V full scale, 13 bit result including sign with 10 bit resolution.
- optional configurations with unity gain instrumentation amplifier for 8 or 16 differential inputs; 13 bit result including sign with 10 or 13 bit resolution.
- single-ended or differential current inputs via user installed shunt resistors.
- temperature compensated high-precision reference for 13 bit resolution including sign.
- uses standard DCE power supplies.
- standard hardware and software interface to the DCE-BUS.
- selectable card address.
- single 100 x 160 mm eurocard format.

## 7.6.3. FUNCTIONAL BLOCK DIAGRAM



## 7.6.4 SYSTEM DESIGN PARAMETERS

### 7.6.4.1 Hardware Configuration

The functional block diagram in Section 7.6.3 illustrates the configurations for all available versions of RWC-AI modules. The instrumentation amplifier is present for the differential input versions only (/8D, /8DH, /16D, /16DH). The multiplexers S1 to S4 each have eight channels, and are installed according to the input channel requirements. The different configurations of the RWC-AI modules are as follows :

a) RWC-AI/16S

This provides 16 single-ended voltage input channels, and produces a 13-bit result including sign, with 10-bit resolution.

It has jumpers 1 - 3, 8 - 9 and multiplexers S1, S2 already installed.

b) RWC-AI/32S

This version provides 32 single-ended voltage input channels and produces a 13-bit result including sign, with 10-bit resolution.

It has jumpers 1 - 3, 2 - 3, 8 - 9 and multiplexers S1, S2, S3, S4 already installed.

c) RWC-AI/8D

This version provides 8 differential voltage input channels and produces a 13-bit result including sign, with 10-bit resolution.

It has an instrumentation amplifier adjusted for unity gain, jumpers 1 - 4, 2 - 5, 7 - 9, and multiplexers S1, S3 already installed.

d) RWC-AI/8DH

Same as for RWC-AI/8D, but with 13 bit resolution

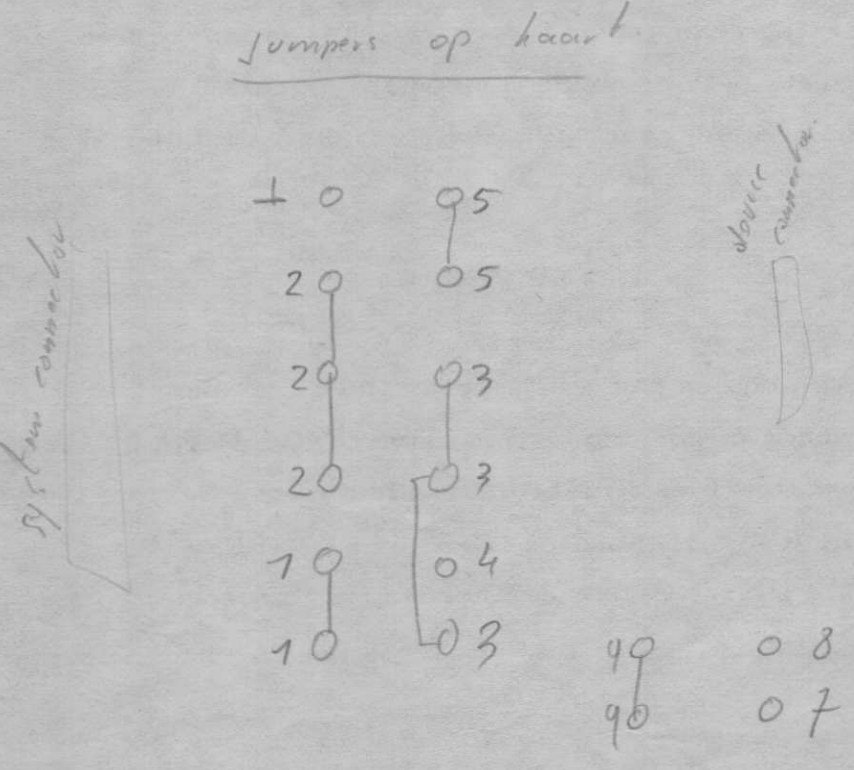
e) RWC-AI/16D

This version provides 16 differential voltage input channels and produces a 13-bit result including sign, with 10-bit resolution.

It has an instrumentation amplifier adjusted for unity gain, jumpers 1 - 4, 2 - 5, 7 - 9, and multiplexers S1, S2, S3, S4 already installed.

f) RWC-AI/16DH

Same as for RWC-AI/16D, but with 13 bit resolution



7.6.4.2 Programming Specifications

The RWC-AI modules are addressed via the standard DCE bus interface. Programming specifications for driving the DCE-BUS are given in Section 4.1.

RIC Initialization

The RIC on the RWC-AI modules should be initialized by writing the control word 92H to the RIC Command Register. This configuration provides a 16-bit data path from the A/D converter device to the DCE-BUS via RIC Ports 0 and 1; and a 8-bit path from the DCE-BUS to the analog channel select multiplexers via RIC Port 2.

The 16-bit data path is used for 13 bits of data representing the digital value of the selected analog channel, and 2 control bits from the A/D converter. The 8-bit data path provides the control signals for selecting the analog channel and generating the start signal for the A/D converter.

RIC Device Addresses

The RIC on the RWC-AI modules has 3 data ports and a command register. Different modes of communication between RIC Ports 0, 1,2 and the DCE-BUS data path are established depending on the Device Address received by the RWC-AI modules from the DCE-BUS. The following table shows the Device Addresses needed for different communication modes.

| DEVICE ADDRESS (HEX) | $\overline{RD}$ | $\overline{WR}$ | OPERATION |
|---|---|---|---|
| Y0 | 0 | 1 | RIC Port 0 → DCE Data Bus |
| Y1 | 0 | 1 | RIC Port 1 → DCE Data Bus |
| Y2 | 0 | 1 | Invalid Operation |
| Y3 | 0 | 1 | Illegal Condition |
| Y0 | 1 | 0 | Invalid Operation |
| Y1 | 1 | 0 | Invalid Operation |
| Y2 | 1 | 0 | DCE Data Bus → RIC Port 2 |
| Y3 | 1 | 0 | DCE Data Bus → RIC Command Register |
| ZX | X | X | RIC Data Bus in 3-state |

DATA → see table 7.6.2 of 7.6.3

Notes:

1. Y is the card address select switch setting in hex (1 to F).
2. Z is any number other than Y.
3. X means don't care
4. RDRWC and WRRWC software routines provide the $\overline{RD}$ and $\overline{WR}$ signals accordingly.
5. Bits 2 and 3 in the low-order byte of the Device Addresses are don't care states.

Table 7.6.1 : Device Address Table for RWC-AI Modules

Format of Data

The digital output from the A/D converter corresponding to a selected analog input signal is input to the DCE-BUS via RIC Ports 0 and 1. The digital result from the converter consists of 13 bits. 2 of the bits of RIC Port 0 are used for status signals from the A/D converter. Input signal allocation for RIC Port 0 and 1 bits are as follows:

| | | | |
|---|---|---|---|
| Port 0 : | b0 | = | A/D converter busy flag indicating when a conversion is in progress. |
| | b1 | = | A/D converter over-range flag indicating that the analog voltage input is outside specified range. |
| | b2 | = | not used |
| | b3- b7 | = | A/D output data bits 0 - 4 |
| Port 1 : | b0- b7 | = | A/D output data bits 5 - 12 |

The START signal to the A/D converter, and 7 control signals for selecting an analog input channel are sent from the DCE-BUS to RIC Port 2. The format of the control word is as follows:

| | | | | |
|---|---|---|---|---|
| Port 2 : | b0- b2 | = | A0-A2 : | input channel select signals (decoded within each multiplexer to select 1 out of 8 analog inputs) |
| | b3 | = | E1 : | multiplexer S1 enable |
| | b4 | = | E2 : | multiplexer S2 enable |
| | b5 | = | E3 : | multiplexer S3 enable |
| | b6 | = | E4 : | multiplexer S4 enable |
| | b7 | = | START: | start pulse to the A/D converter to initiate the conversion. |

Interpretation of Data

The A/D converter on the RWC-AI modules gives a 13-bit digital result in two's complement form. This holds true for both the

10-bit as well as 13-bit resolution configurations. For the 10-bit version, the 3 low order bits of the 13-bit result should not be depended upon for accuracy. Such an arrangement allows software compatibility between results from the two versions of the module.

Since the 13-bit digital result is in two's complement form, the most significant bit acts as the sign bit. If this bit is set, the result is negative (0 to -2.5V analog input); if it is clear, the result is positive (0 to +2.5V analog input). When the sign bit is set, the actual value of the negative result is given by the remaining 12-bits in two's complement form. When the sign bit is clear, the value of the positive result is given by the remaining 12 bits in the normal form. This is illustrated in the figure below:

| ANALOG INPUT | | 13-BIT DIGITAL OUTPUT | |
|---|---|---|---|
| +2.5V | ⟷ | 0 1111111111111 | 4095 |
| . | | . | |
| . | | . | |
| . | | . | |
| 0V | ⟷ | 0 0000000000000 | 0 |
| | | 1 1111111111111 | 8191 |
| . | | . | |
| . | | . | |
| . | | . | |
| -2.5V | ⟷ | 1 0000000000000 | 4096 |

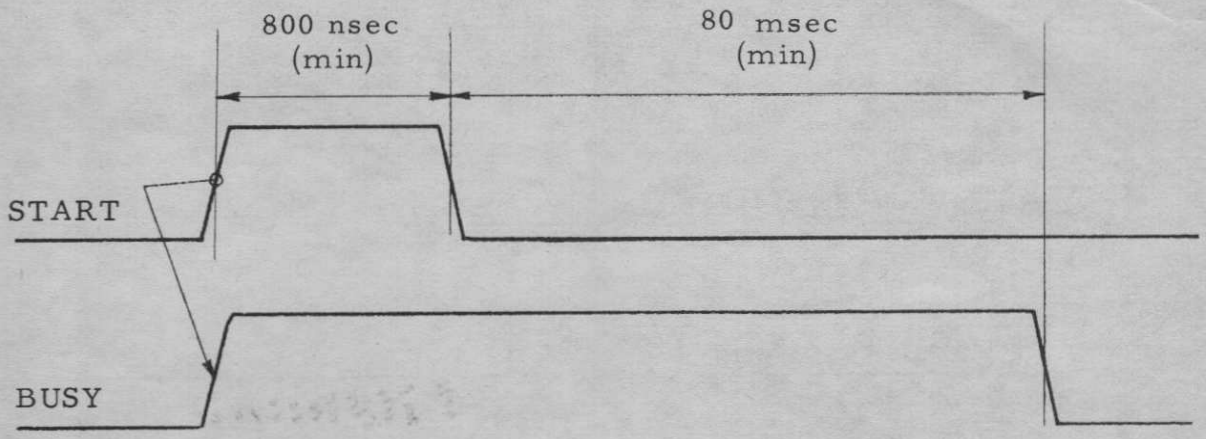
The digital output in its normal form is suitable for performing arithmetic operations etc. where a sign capability is needed. However, it can be interpreted to suit specific requirements.

For example, by complementing the sign bit (by software) it is possible to have a range of all zeros to all ones in the digital result, corresponding to the analog input range of -2.5V to +2.5V. In such a case the 13th bit

in the result also becomes a data bit giving a range of digital values from 13 zeros to 13 ones.

Special Considerations

The analog to digital conversion procedure is initiated by giving a START pulse to the A/D converter (via RIC Port 2 bit 7). The timing diagram below shows the sequence of operation:




The rising edge of the START signal produces the BUSY output signal from the A/D converter. However, the actual conversion does not commence until the falling edge of the START signal. BUSY is a status signal which when high indicates that a conversion is in progress. The RWC-AI16 module design allows this BUSY signal to be used as a software polled flag (via RIC Port 0 bit 0), or as an interrupt request generator at the end of a conversion. Interrupt driven operation of the RWC-AI modules allow the DCE processor to carry out other functions while an A/D conversion is in progress.

The A/D converter provides an over-range flag OVRG via RIC Port 0 bit 1. This when true indicates that the analog input signal was outside the specified range ( $\pm$ 2.5V).

The digital result read from the RWC-AI modules is valid only if both BUSY and OVRG signals are low.

## RWC-AI RIC / DCE-BUS Protocol

### Initialization

The RWC-AI module RIC should first be initialized by writing control word 92H to its Command Register. This will configure RIC Ports 0, 1, 2 in the required modes. All analog input channels should then be de-selected by writing control word 00 to RIC Port 2. The A/D converter does not have a RESET input; therefore, it may start-up with a random conversion in progress. One way to clear the A/D converter is to select an arbitary input channel, perform a conversion as described below, and to wait till the BUSY line goes low. The RWC-AI is then ready for normal operation.

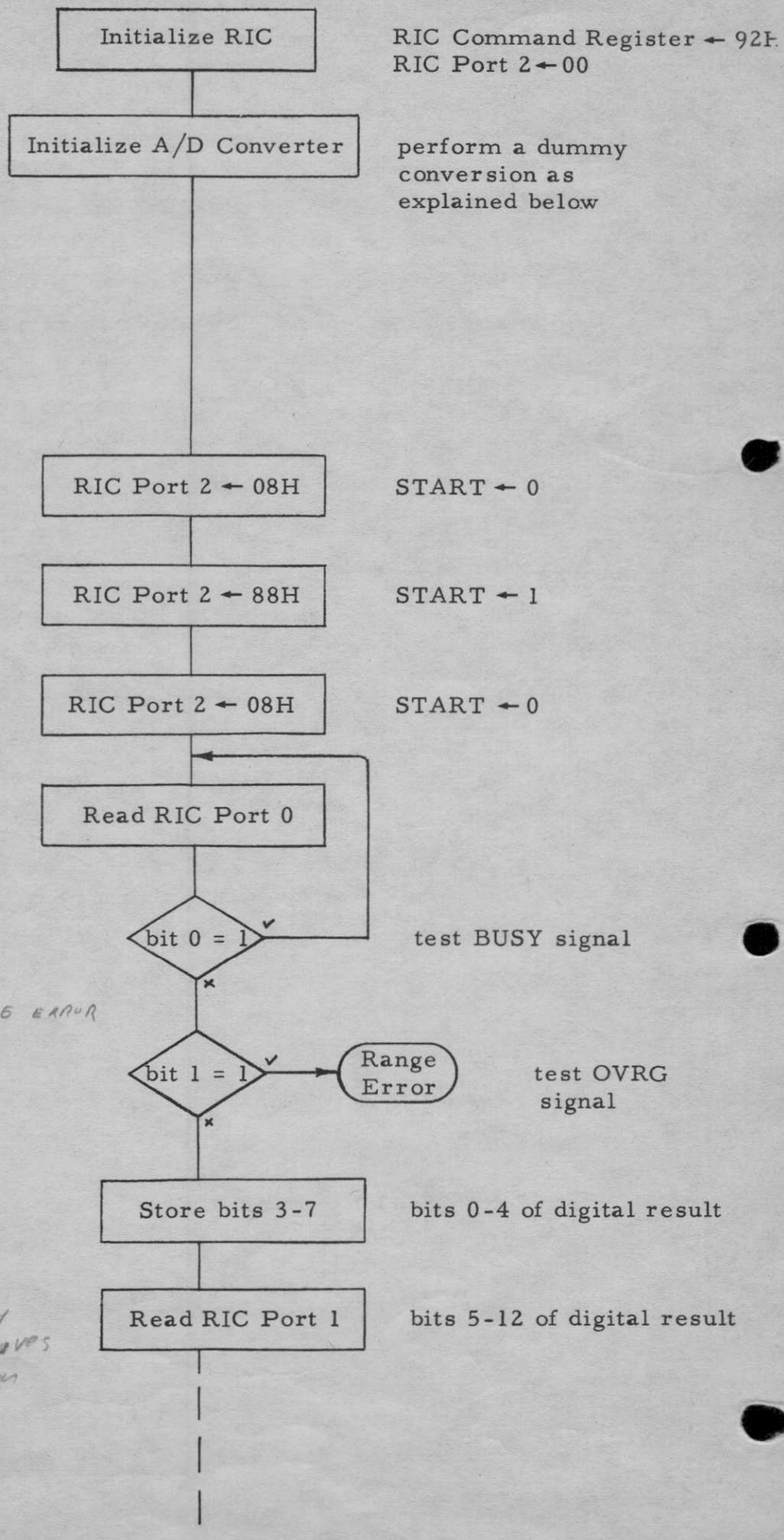
### A/D Conversion

In order to initiate an A/D conversion, select the required analog input by writing the appropriate channel select control word with bit 7 = 0 (START bit) to RIC Port 2. See Table 7.6.2 and 7.6.3 for values of channel select control words. Do two more write operations to RIC Port 2 with bit 7 = 1 and then 0, while keeping the other bits unchanged. This sequence will pulse the START input to the A/D converter and initiate the conversion. It is important to note that the START bit should not be sent at the same time as the channel select address.

The conversion will be finished when the BUSY line goes low. Therefore, read RIC Port 0 until bit 0 becomes zero. Next test the OVRG flag (bit 1). If zero, the conversion results are correct and the low-order 5 bits have already been read from RIC Port 0. Then read the high-order 8 bits from RIC Port 1.

The complete software controlled conversion sequence is given below:

Initialization




Example of a conversion on analog input at connector pin 1 (channel select control word = 08H)

Basic.

OUT Y2, #08

OUT Y2, #88

OUT Y2, #08

of

WAIT Y0, 01, 01

L = INP (Y0)

IF L AND 2 = 2 THEN OVRG ERROR

H = INP (Y1)

reading only RIC port 1 gives 8 bit resolution

See Section 7.6.5 for a programming example.

If a RWC-AI module is configured to generate an interrupt when BUSY goes low, the interrupt service routine should test the OVRG flag, and if zero read the digital output.

All valid channel select control words are specified in Tables 7.6.2 and 7.6.3.

Note: For single-ended inputs, a control word value which simultaneously enables more than one multiplexer (more than one of the bits E1, E2, E3, E4 high) should never be used. Such an occurance will give incorrect results and possibly cause damage to the multiplexers. Similarly for differential inputs, only one of the multiplexer pairs S1, S3 or S2, S4 should be enabled simultaneously.

| $U_{in}$ | X |
|---|---|
| +2,5V | 4095 |
| | ⋮ |
| 0 | 0 |
| | |
| -2,5V | -4095 |

L = INP(Y0)
H = INP(Y1)

X = H SHL 5 + L SHR 3

IF X > &HFFF THEN X = X - &H1FFF

| Device connector pin number (Analog Inputs) | Channel select control word in Hex (RIC Port 2 bits 6-0) | Multi-plexer used | Socket pin number of shunt resistor pad | | | |
|---|---|---|---|---|---|---|
| | | | L1 | L2 | L3 | L4 |
| 1 WIT | 08 | S1 | 1 | | | |
| 2 BRUIN | 09 | | 3 | | | |
| 3 GROEN | 0A | | 5 | | | |
| 4 GEEL | 0B | | 7 | | | |
| 5 GRIJS | 20 | S3 | | | 16 | |
| 6 ROSE | 21 | | | | 14 | |
| 7 BLAUW | 22 | | | | 12 | |
| 8 ROOD | 23 | | | | 10 | |
| 9 ZWART | 10 | S2 | | 1 | | |
| 10 PAARS | 11 | | | 3 | | |
| 11 GRIJS-ROSE | 12 | | | 5 | | |
| 12 ROOD-BLAUW | 13 | | | 7 | | |
| 13 WIT-GROEN | 40 | S4 | | | | 16 |
| 14 BRUIN-GROEN | 41 | | | | | 14 |
| 15 WIT-GEEL | 42 | | | | | 12 |
| 16 GEEL-ROOD BRUIN | 43 | | | | | 10 |
| 20 ROSE-BRUIN | 0C | S1 | 2 | | | |
| 21 WIT-BLAUW | 0D | | 4 | | | |
| 22 BRUIN-BLAUW | 0E | | 6 | | | |
| 23 WIT-ROOD | 0F | | 8 | | | |
| 24 BRUIN-ROOD | 24 | S3 | | | 15 | |
| 25 WIT-ZWART | 25 | | | | 13 | |
| 26 BRUIN-ZWART | 26 | | | | 11 | |
| 27 GRIJS-groen | 27 | | | | 9 | |
| 28 GEEL-GRIJS | 14 | S2 | | 2 | | |
| 29 ROSE-GROEN | 15 | | | 4 | | |
| 30 GEEL-ROSE | 16 | | | 6 | | |
| 31 GROEN-BLAUW | 17 | | | 8 | | |
| 32 GEEL-BLAUW | 44 | S4 | | | | 15 |
| 33 GROEN-ROOD | 45 | | | | | 13 |
| 34 GEEL-ROOD | 46 | | | | | 11 |
| 35 GROEN-ZWART | 47 | | | | | 9 |
| 17 WIT-GRIJS<br>18 GRIJS-BRUIN<br>19 WIT-ROSE<br>36 GEEL-ZWART<br>37 GRIJS-BLAUW | common analog ground | | | | | |

Table 7.6.2 : Single-ended Analog Input Configurations

This table shows the relationship between analog input signals via the device connector pins, control word value for software selection of each input channel, multiplexer and shunt resistor (if required) configuration for each input channel. The pin numbers for the shunt resistor pad sockets are as defined in the block diagram of Section 7.6.3.

| N | Analog Input channel number | Device connector pin pairs for differential input signal connection | Channel select control word in Hex (RIC Port 2 bits 6-0) MCW | Multiplexers used |
|---|---|---|---|---|
| 0 | 1 | 1- 5 | 28 | |
| 1 | 2 | 2- 6 | 29 | |
| 2 | 3 | 3- 7 | 2A | |
| 3 | 4 | 4- 8 | 2B | S1 and S3 |
| 4 | 5 | 20-24 | 2C | |
| 5 | 6 | 21-25 | 2D | |
| 6 | 7 | 22-26 | 2E | |
| 7 | 8 | 23-27 | 2F | |
| 8 | 9 | 9-13 | 50 | |
| 9 | 10 | 10-14 | 51 | |
| 10 | 11 | 11-15 | 52 | |
| 11 | 12 | 12-16 | 53 | |
| 12 | 13 | 28-32 | 54 | S2 and S4 |
| 13 | 14 | 29-33 | 55 | |
| 14 | 15 | 30-34 | 56 | |
| 15 | 16 | 31-35 | 57 | |

32*(N/8+1)+N+8

Table 7.6.3 : Differential Analog Input Configurations

This table gives analog input signal connections, and channel select control word combinations for 16 differential input versions of the RWC-AI16 module. The 8 differential input versions must only use channels 1 to 8. The channel numbering is arbitary.

$MCW = 32*(N/8+1)+N+8$

7.6.4.3 User Options

Interrupt Generation Jumpers

Jumper network 10 - 11 - 12 allows the user to connect the $\overline{\text{BUSY}}$ output signal of the A/D converter to interrupt request lines EXINTR (10 - 12) or IN7 (10 - 11) on the DCE-BUS.

Shunt Resistors for Current Input

The RWC-AI modules are normally configured for measuring voltage inputs. However, resistor pads are provided to enable the user to connect shunt resistors for current inputs. The user should solder 16-pin sockets to these resistor pads and install accurate shunt resistors on component carriers. The resistor values should be selected to produce a voltage in the range $\pm$ 2.5V. The Functional Block Diagram of the module (Section 7.6.3) shows the positions of these shunt resistor pads L1, L2, L3 and L4 as well as the pin numbers for their sockets.

Shunt resistor pads L1, L2, L3, L4 are associated with multiplexers S1, S2, S3, S4 respectively.

Shunt resistor installation procedures for the different versions of the RWC-AI modules are as follows:

a) 16 single-ended current inputs

The RWC-AI/16S configuration can be used for this purpose. The voltage input signals are passed through multiplexers S1 and S2; therefore, resistor pads L1 and L2 should be used. Solder two sockets at these locations. Install the shunt resistors on component carriers, with a common link from pins 9 to 16 on each one. This provides a common ground at pin 9 for the resistors on each carrier.

b) 32 single-ended current inputs

The RWC-AI/32S configuration must be used for this. The voltage input signals are passed through all four multiplexers, and therefore all four resistor pads should be used. Solder four sockets and install shunt resistors on component carriers. Common links from pins 9 to 16 should be provided on the carriers for sockets L1 and L2. Links from pins 1 to 8 should be provided on the carriers for sockets L3 and L4. These links provide a common ground for the resistors on each carrier.

c) 8 differential current inputs

RWC-AI/8D or 8/DH can be used for this. The differential voltage inputs are passed through multiplexers S1 and S3. Solder a socket in the position exactly between the L1 and L3 resistor pads, and install the shunt resistors on a component carrier. Since this is a differential input scheme, none of the pins of the component carrier should be linked for grounding purposes.

d) 16 differential current inputs

The RWC-AI/16D or /16DH must be used here. The differential voltage inputs are passed through multiplexer pairs S1, S3 and S2, S4. Solder two sockets in the positions exactly between pads L1, L3 and L2, L4. Install shunt resistors on component carriers, without any common links for grounding.

7. 6. 4. 4. Module Connector Definitions

System Connector

see Section 6. 1.4 for the pin definitions.

Device Connector

All the analog input signals are provided via the Device Connector. Pin numbers 1 - 16 and 20 - 35 provide 32 input channels. See Table 7. 6. 2 for a summary of the Device Connector pins for the input channels, and the associated resistor pad pin numbers and channel select control words.

Analog Input Connections

Table 7. 6. 2 summarizes all the possible voltage/current input channels in association with the multiplexers and shunt resistor pads.

Input channel connections for the different versions of the RWC-AI modules are as follows :

a) 16 single-ended inputs
Connect to Device Connector pins 1 - 4, 9 - 12, 20 - 23, and 28 - 31. Only S1 and S2 multiplexers are used.

b) 32 single-ended inputs
Connect to Device Connector pins 1 - 16 and 20 - 35. All four multiplexers are used.

c) 8 differential inputs
Connect the 8 differential input signals between the following pairs of pins on the Device Connector : 1 - 5, 2 - 6, 3 - 7, 4 - 8,

20 -24, 21 - 25, 22 - 26, 23 - 27, (see Table 7.6.3 - first 8 channels). Multiplexer pair S1 and S3 are used.

d) 16 differential inputs

Connect the 16 differential input signals between pairs of pins on the Device Connector, as defined in Table 7.6.3.

Analog Input Requirements

The analog input signals to the RWC-AI modules can be voltages or currents. For correct operation, the voltage to be converted should not exceed $\pm$ 2.5V. Therefore, if current inputs are used, the shunt resistors should be selected to produce a voltage input within the above limits.

The frequency of the analog input signals in the 32 single-ended input configuration may not exceed 0.3 Hz. For the other input configurations, this value may be slightly higher due to the lower sampling rates.

All analog input signals must be twisted pairs or screened wires.

In differential input modes, the DCE system ground and the analog signal source ground must be joined together.

7.6.4.5 Operational Requirements

Power Requirement

Each RWC-AI requires three power supplies from the DCE-BUS. The values given below are for the quiescent state. Active state values are typically 20% higher for all configurations.

| | | |
|---|---|---|
| +12V | : | 75mA |
| +5V | : | 175mA |
| -5V | : | 60mA |

Environmental Requirements

| | | |
|---|---|---|
| Operating temperature | : | 0°C to 55°C |
| Storage temperature | : | -25°C to +85°C |
| Relative humidity | : | 95% noncondensing |

Bus Loading

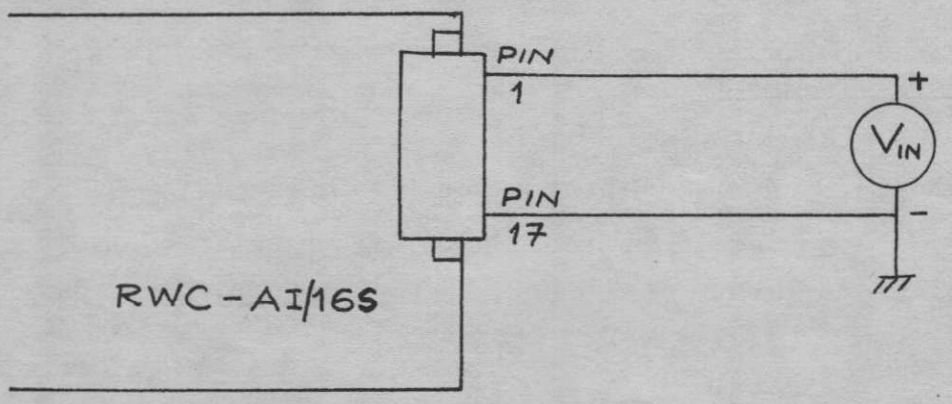
The RWC-AI modules present 1 unit-load to the DCE-BUS (see Section 4.4).

## 7.6.5. TEST PROCEDURE

This section defines a simple test configuration and a test program for performing a basic functional test on the RWC-AI/16S module. Users are advised to carry out such a test procedure when necessary to establish the correct functioning of a module. The test program also provides a good example of RWC-AI module driver software.

Test Configuration

The following test program relates to the test configuration below. It assumes a RWC-AI/16S module, with an analog voltage input connected across pins 1 and 17 on the Device Connector.



## RWC-AI/16S Test Program

```
V2.0 DCE=2
P=1

P=2
  0000                    ; THIS IS A SIMPLE PROGRAM FOR TESTING THE
  0000                    ; STANDARD RWC-AI16 WITH CARD ADDRESS SELECT
  0000                    ; SWITCH SET TO 'E', USING THE DCE DEVELOPMENT
  0000                    ; SYSTEM WITH DCE-2 UTILITY VERSION 2.0 AND
  0000                    ; RESIDENT DCE ASSEMBLER.
  0000                    ; THE PROGRAM READS AN ANALOG VOLTAGE CONNECTED
  0000                    ; ACROSS DEVICE CONNECTOR PINS 1 AND 17, AND
  0000                    ; TYPES THE EQUIVALENT DIGITAL RESULT AS 4 HEX
  0000                    ; DIGITS. THE HIGH-ORDER 13 BITS OF THE PRINTED
  0000                    ; VALUE WILL CONTAIN THE 13 BIT DIGITAL RESULT.
  0000                    ; THE LOW-ORDER 3 BITS WILL BE ZERO.
  0000                    ; THE PROGRAM IS ENTERED FROM THE UTILITY AND
  0000                    ; RETURNS TO THE UTILITY AFTER EACH CONVERSION.
  0000                                ;
  0000                                ;
  031E          RDRWC:  EQU     031E
  0349          WRRWC:  EQU     0349
  061F          TCRLF:  EQU     061F
  05FD          TADDR:  EQU     05FD
  0000                                ;
  1000                  ORG     1000
  1000                                ;
  1000 CD2C10   BEGIN:  CALL    INIT  ; INITIALIZE RIC
  1003 CD4A10           CALL    START ; A/D CONVERTER INITIALIZATION
  1006                                ;   VIA A DUMMY CONVERSION.
  1006 CD4110   LOOPA:  CALL    LDFLG ; LOAD STATUS FLAGS
  1009 E601             ANI     01
  100B C20610           JNZ     LOOPA ; LOOP TILL BUSY = 0
  100E                                ;
  100E                                ; END OF INITIALIZATION
  100E                                ;
  100E CD4A10   CONV:   CALL    START ; DO ACTUAL CONVERSION
  1011 CD4110   LOOPB:  CALL    LDFLG ; LOAD STATUS FLAGS
  1014 47               MOV     B,A   ; STORE
  1015 E601             ANI     01
  1017 C21110           JNZ     LOOPB ; LOOP TILL BUSY = 0
  101A                                ; TEST FOR OVER-RUN
  101A 3E02             MVI     A,02
  101C A0               ANA     B
  101D C22510           JNZ     ERR   ; IF OVER-RUN, PRINT 'FFFF'
  1020 68               MOV     L,B   ; STORE RESULT BITS 0-4
  1021                                ;  LOWER 3 BITS ALREADY CLEAR
  1021 CD5F10           CALL    RDPRT ; READ REST OF RESULT AND PRINT
  1024 C9               RET           ; RETURN TO UTILITY
```

```
1025                                        ;
1025                                        ; ERROR EXIT
1025 21FFFF      ERR:   LXI     H,0FFFF
1028 CD6810             CALL    PR          ; PRINT 'FFFF'
102B C9                 RET                 ; RETURN TO UTILITY
102C                                        ;
102C                                        ; SUBROUTINES
102C                                        ;
102C                                        ; RIC INITIALIZATION
102C 3EE3        INIT:  MVI     A,0E3
102E 32011C             STGI    1           ; SELECT RIC COMMAND REGISTER
1031 3E92               MVI     A,92
1033 CD4903             CALL    WRRWC       ; CONFIGURE RIC
1036                                        ;
1036 3EE2        DSABL: MVI     A,0E2
1038 32011C             STGI    1           ; SELECT RIC PORT 2
103B 3E00               MVI     A,00
103D CD4903             CALL    WRRWC       ; DISABLE ALL ANALOG INPUTS
1040 C9                 RET
1041                                        ;
1041                                        ; LOAD FLAGS FROM RIC PORT 0
1041 3EE0        LDFLG: MVI     A,0E0
1043 32011C             STGI    1           ; SELECT RIC PORT 0
1046 CD1E03             CALL    RDRWC       ; READ PORT
1049 C9                 RET
104A                                        ;
104A                                        ; A/D CONVERSION ROUTINE
104A 3EE2        START: MVI     A,0E2
104C 32011C             STGI    1           ; SELECT RIC PORT 2
104F 3E08               MVI     A,08
1051 CD4903             CALL    WRRWC       ; SELECT A CHANNEL
1054                                        ;   WITH START BIT = 0.
1054 3E88               MVI     A,88        ; SET START BIT = 1
1056 CD4903             CALL    WRRWC
1059 3E08               MVI     A,08        ; RESET START BIT
105B CD4903             CALL    WRRWC
105E C9                 RET
105F                                        ;
105F                                        ; READ HIGH ORDER 8 BITS FROM
105F                                        ;   PORT 1 AND PRINT ANSWER.
105F 3EE1        RDPRT: MVI     A,0E1
1061 32011C             STGI    1           ; SELECT RIC PORT 1
1064 CD1E03             CALL    RDRWC       ; READ PORT
1067 67                 MOV     H,A         ; STORE IN H REGISTER
1068                                        ;
1068 CD1F06      PR:    CALL    TCRLF       ; PRINT C/R L/F
106B CDFD05             CALL    TADDR       ; PRINT DIGITAL RESULT IN H,L
106E C9                 RET
                        END
```

## 7.6.6 ORDERING INFORMATION

RWC-AI/16S : 16 single-ended inputs;
13 bit result including sign, with 10-bit resolution

RWC-AI/32S : 32 single-ended inputs;
13-bit result including, sign, with 10-bit resolution

RWC-AI/8D : 8 differential inputs;
a unity gain instrumentation amplifier;
13-bit result including sign, with 10-bit resolution

RWC-AI/8DH : same as RWC-AI/8D but giving a 13-bit result including sign, with a 13-bit resolution

RWC-AI/16D : 16 differential inputs;
a unity gain instrumentation amplifier;
13-bit result including sign, with 10-bit resolution

RWC-AI/16DH : same as RWC-AI/16DH but giving a 13-bit result including sign, with 13-bit resolution.