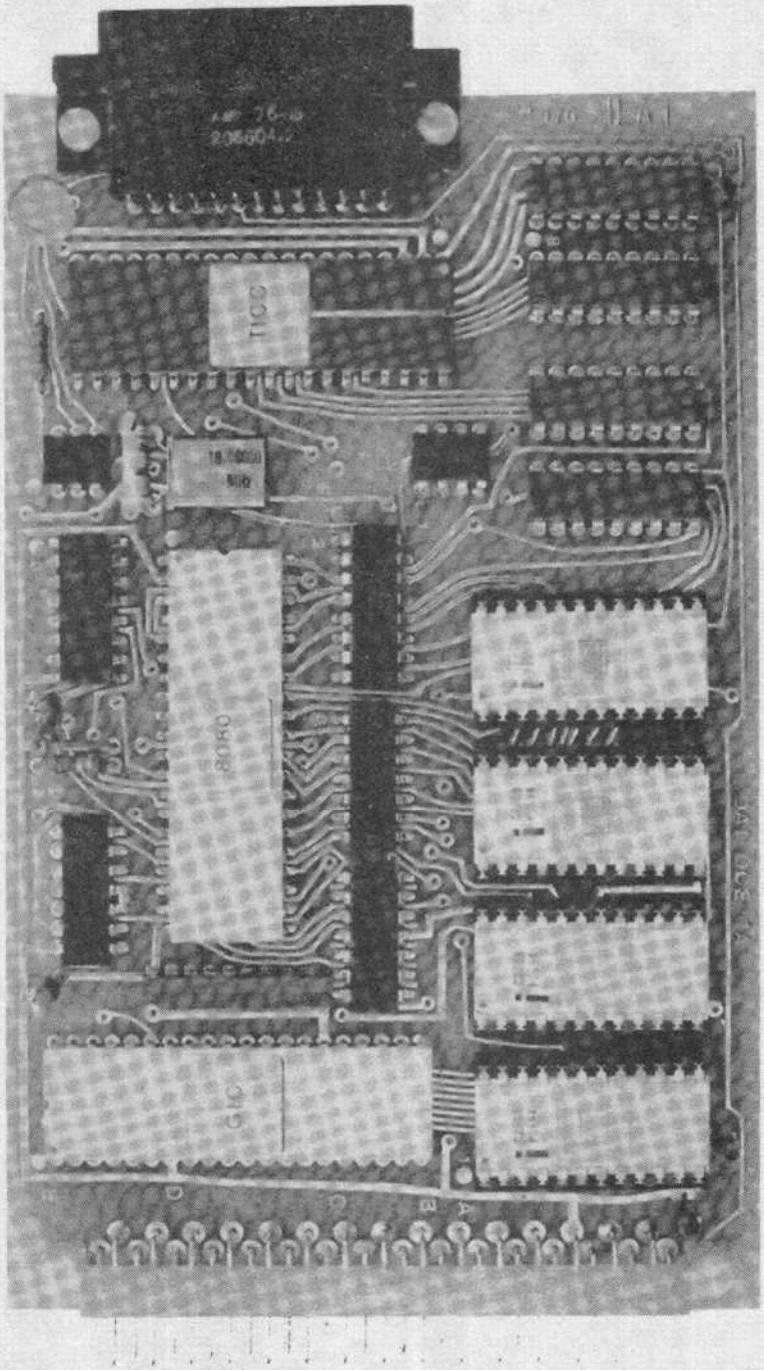


DCE-1, Actual Size

6. DCE PROCESSOR MODULES

6.1 GENERAL SPECIFICATIONS

The DCE single eurocard (100 x 160 mm) microcomputer family provides the digital computing power of the popular 8080 microprocessor enhanced by fully implemented serial and parallel I/O capability, five independent interval timers and fully vectored interrupts. The opto-isolated serial communication interface has programmable Baud rates, and may be interrupt driven. The interval timers function independently of the CPU, and provide 64 microsecond resolution with crystal accuracy. There are 40 parallel I/O lines, 24 of which can be programmed as input, output, bi-directional or handshaking ports, with automatic handshake control signals.

All DCE processor modules can be interchanged without system modification. Source programs written for one DCE processor need only be re-assembled for any other DCE processor, and no back-panel or connector re-wiring is necessary.

DCE processor modules provide a standard hardware and software interface to the family of "Real-World" interface modules via the DCE-BUS. They plug into the parallel-wired DCE eurocard racks and are package compatible with all the support modules. Each DCE processor is tested and fully burned-in before delivery.

The exchange of data and control information between the DCE processor modules and the interface modules is achieved via the DCE-BUS. The DCE-BUS is realized by configuring the GIC ports on the DCE processor module in a specific manner. Complete specifications of the DCE-BUS are given in Section 4.

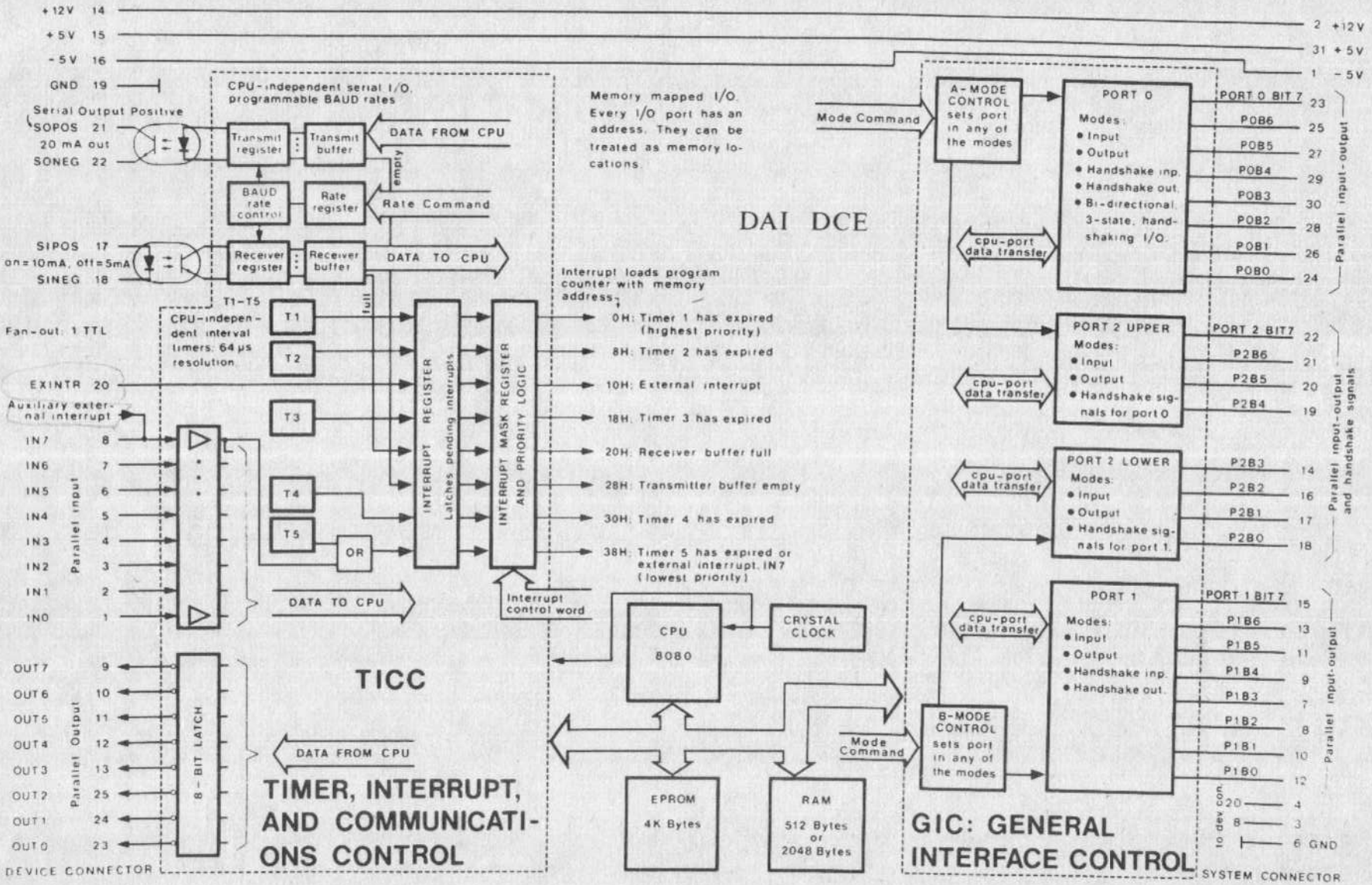


Figure 6-1. DCE Detailed Block Diagram

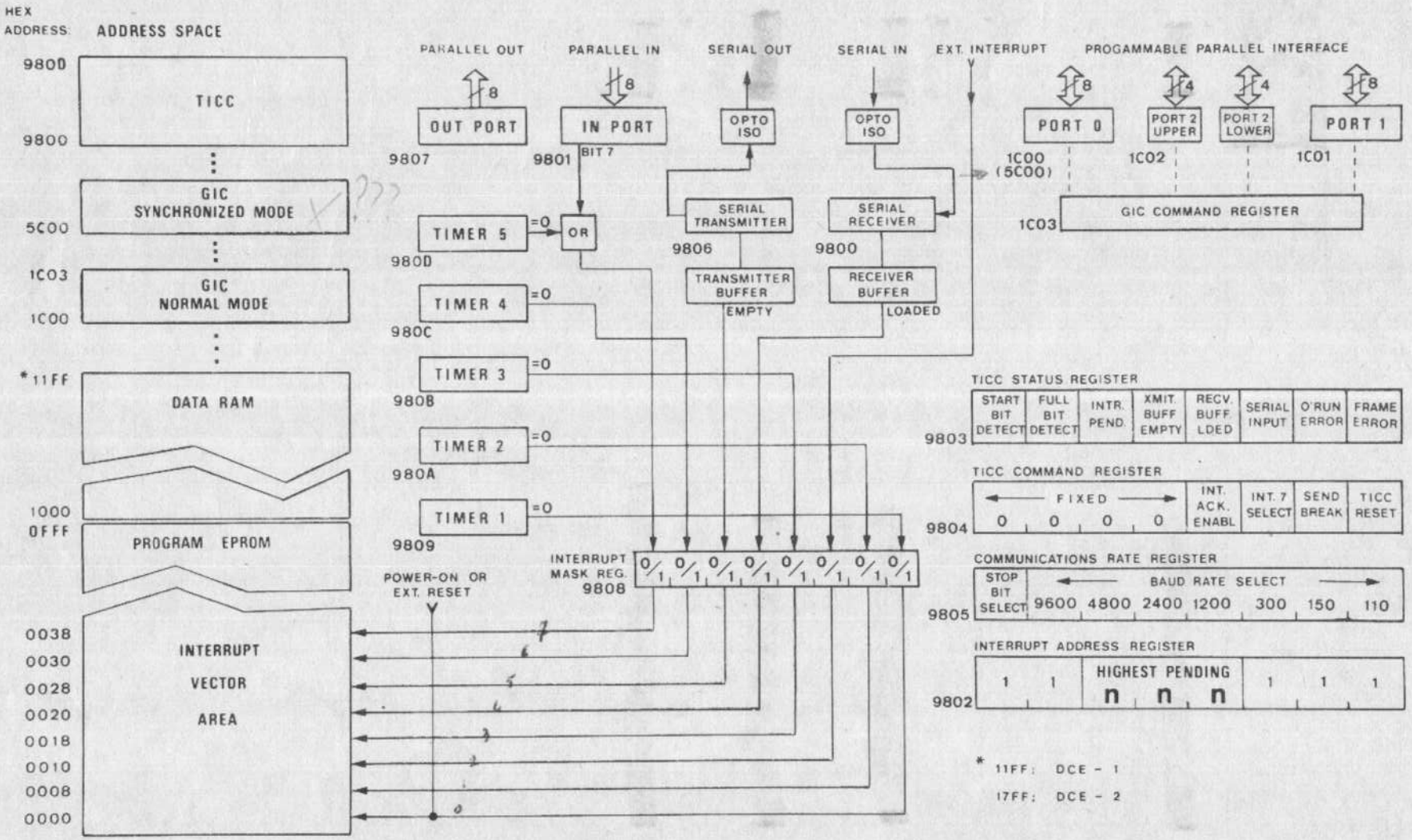


Figure 6-2. Memory and Register Diagram

REGISTER/PORT	ADDRESS (HEX)	
	DCE-1 DCE-2	DCE-1A DCE-2A DCE-X
GIC Command Register	1C03	FF03
GIC Port 0	1C00	FF00
GIC Port 1	1C01	FF01
GIC Port 2	1C02	FF02
GIC Port 0 (Sync. Mode)	5C00	FF08
TICC Serial Receiver	9800	FF10
TICC Parallel Input Port	9801	FF11
TICC Interrupt Address Register	9802	FF12
TICC Status Register	9803	FF13
TICC Command Register	9804	FF14
TICC Communications Rate Register	9805	FF15
TICC Serial Transmitter	9806	FF16
TICC Parallel Output Port	9807	FF17
TICC Interrupt Mask Register	9808	FF18
TICC Timer 1	9809	FF19
TICC Timer 2	980A	FF1A
TICC Timer 3	980B	FF1B
TICC Timer 4	980C	FF1C
TICC Timer 5	980D	FF1D

Table 6-1 : GIC and TICC Register Addressing for Different DCE Processor Modules

6.1.1 Detailed DCE Block Diagram

Figure 6-1 shows the detailed block diagram for 8080 based DCE modules. The PROM and RAM memory capacity indicated is applicable to DCE-1, 1A, 2, 2A modules only. The memory expandable DCE-X has no memory provided on the module. A flat-cable X-BUS connector is provided on the DCE-X for connecting memory modules to provide upto 64K bytes of memory.

6.1.2 DCE Memory and Register Diagram

Figure 6-2 shows the general memory and register diagram for DCE-1 and DCE-2 modules. The TICC and GIC register addresses, PROM memory addresses and the RAM memory start address are the same for DCE-1 and DCE-2. The TICC and GIC register addresses for DCE-X, 1A, 2A are different from those in Figure 6-2. Table 6-1 gives the addressing for the different processor modules. Register address differences between the different DCE processor modules are automatically resolved by the resident assembler (UAE) in the DCE-DM development system, when translating TICC and GIC macros. For this reason, users are advised to use the TICC and GIC macros specified in Section 5.2, when accessing the TICC and GIC registers.

6.1.3 DCE Program Memory

The DCE modules that accept program memory (DCE-1, DCE-2 etc.) have sockets provided for erasable and electrically reprogrammable read-only memory (EPROM). The sockets accommodate the 2708 1K byte, the 2716 2K byte, or pin compatible devices. These are packaged in 24 pin dual-in-line case with a transparent lid, which allows the user to expose the memory chip to ultraviolet light to erase the bit-pattern. The EPROMs can then be re-programmed. The erase-rewrite cycle can be repeated as many times as required.

For EPROM programming use DAI's low cost microcomputer development system, the DCE-DM. The DCE-DM system design includes facilities for testing, reviewing, and altering the program before actually programming the PROM. For complete information on these develoment systems refer to the DCE-DM User's Manual.

To erase the bit-pattern, expose the chip through the transparent quartz lid, to high intensity short-wave ultra-violet light at a wave-length of 2537Å. Among recommended ultra-violet light sources are Model UVS and Model S-52 lamps manufactured by Ultra-Violet Products Inc.
The lamps should be used without short-wave filters, and the EPROM to be erased should be placed about one inch away from the lamp tubes for about 20 to 30 minutes.

Figure 6-3 serves as reference for inserting the program memory into the sockets on the DCE card. The diagram shows the card as viewed from the component side. PROM position zero is the low order position referenced by start address 0000. Pin 1 of the PROM is shown as reference for insertion.

Program memory on the DCE-X processor resides on the memory modules connected via the flat-cable X-BUS. These memory modules have switch selectable address ranges, and therefore the program memory can be made to reside in any desired memory range.

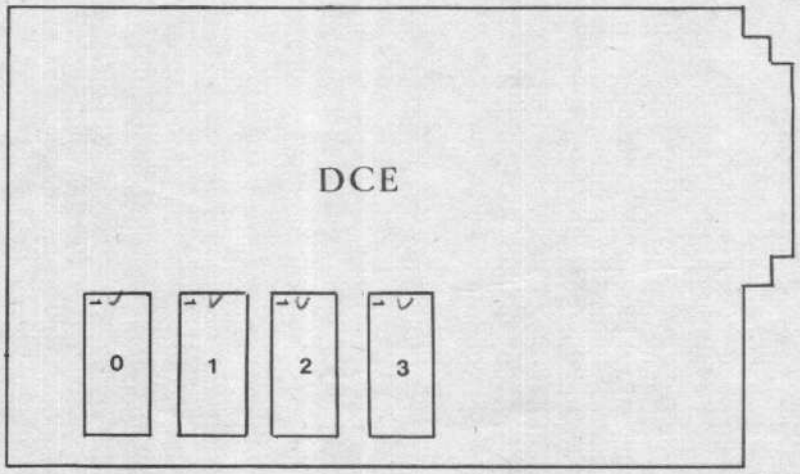


Figure 6-3 : Definition of Program Memory Position and Pin Reference for Insertion of EPROMs

6.1.4 System Connector Pin Definitions

Each DCE processor module has a 31-pin connector at one end. This is the System Connector which plugs into the DCE eurocard racks with the parallel-wired DCE-BUS.

The following pin definitions are valid for all DCE processor modules and DCE-BUS compatible interface modules.

SIGNAL NAME	DESCRIPTION		PIN	PC K1
P0B0	General Interface PORT 0	Bit 0	24	1
P0B1		Bit 1	26	2
P0B2		Bit 2	28	3
P0B3		Bit 3	30	4
P0B4		Bit 4	29	5
P0B5		Bit 5	27	6
P0B6		Bit 6	25	7
P0B7		Bit 7	23	8
P1B0	General Interface PORT 1	Bit 0	12	9
P1B1		Bit 1	10	10
P1B2		Bit 2	8	11
P1B3		Bit 3	7	12
P1B4		Bit 4	9	13
P1B5		Bit 5	11	14
P1B6		Bit 6	13	15
P1B7		Bit 7	15	16
P2B0	General Interface PORT 2	Bit 0	18	17/27
P2B1		Bit 1	17	28
P2B2		Bit 2	16	29
P2B3		Bit 3	14	30
P2B4		Bit 4	19	31
P2B5		Bit 5	20	32
P2B6		Bit 6	21	33
P2B7		Bit 7	22	34
EXINTR*	External Interrupt		4	–
IN7*	Parallel Input Bit 7 (aux. interrupt)		3	–
EXRESET	External Reset (Ground for Reset)		5	–
+12 *	+12V DC		2	–
+ 5 *	+ 5V DC		31	21/22/23/24
- 5 *	- 5V DC		1	–
GND *	Digital and Power Ground		6	18/19/20

* Signal present on both connectors in DCE processors.

6.1.5 Device Connector Pin Definitions

Each DCE processor module has a 25 pin D-type male connector at one end. This is the Device Connector carrying the serial I/O lines and the TICC parallel port lines.

The following pin definitions are valid for all 8080 based DCE processors.

SIGNAL NAME	DESCRIPTION		PIN
SOPOS	Serial Output (Positive)		21
SONEG	Serial Output (Negative)		22
SIPOS	Serial Input (Positive)		17
SINEG	Serial Input (Negative)		18
OUT0	TICC Parallel Output Port	Bit 0	23
OUT1		Bit 1	24
OUT2		Bit 2	25
OUT3		Bit 3	13
OUT4		Bit 4	12
OUT5		Bit 5	11
OUT6		Bit 6	10
OUT7		Bit 7	9
IN0	TICC Parallel Input Port	Bit 0	1
IN1		Bit 1	2
IN2		Bit 2	3
IN3		Bit 3	4
IN4		Bit 4	5
IN5		Bit 5	6
IN6		Bit 6	7
IN7 *	Auxiliary Interrupt, or,	Bit 7	8
EXINTR*	External Interrupt		20
+12 *	+12 from System Connector		14
+ 5 *	+ 5 from System Connector		15
- 5 *	- 5 from System Connector		16
GND *	Signal Ground		19

* Signal present on both connectors.

6.1.6 System Bus Electrical Specifications

SIGNAL	MIN.	TYP.	MAX.	CONDITIONS
GIC Ports 0-2: Input Mode	2.0V		0.8V	Low input High input
Output Mode	2.4V		0.4V	-1.6mA +50μA

6.1.7 Device Connector Electrical Specifications

SIGNAL	MIN.	TYP.	MAX.	CONDITIONS
Parallel Output	3.7V		0.45V	-1.7mA 400μA
Parallel Input	3.3V		0.8V	Low input High input
Input Leakage			±10μA	0-5V input
Serial Input: ON state		10mA 1.2V	15mA 1.3V	Forward Current Forward Voltage
OFF state	2mA 1.0V	5mA 1.1V	20mA	Forward Current Forward Voltage Absolute max. Current
Serial Output: Forward Voltage	0.7V		1.4V 30V	10mA (ON state) Absolute max. (OFF state)
Reverse Voltage			7V	Absolute Maximum
Forward Current			100mA	Absolute Maximum

6.2 DCE-1 PROCESSOR MODULES

6.2.1 FEATURES

- complete 8080 microcomputer system on a single 100 x 160 mm eurocard.
- 512 byte RAM and sockets for 4K or 8K byte EPROM
- opto-isolated serial I/O with programmable Baud rates from 110 to 9600.
- 40 parallel I/O lines; 24 programmable as simple handshaking or bi-directional with automatic handshake control signals.
- 5 independent interval timers providing 64 microsecond resolution with crystal accuracy.
- 8 independently vectored interrupts.

6.2.2 FUNCTIONAL BLOCK DIAGRAM

Figure 1-2 on page 1-6 shows the general block diagram. Figure 6-1 shows a detailed functional block diagram. RAM memory occupies address space 1000H to 11FFH for DCE-1, and D000H to D1FFH for DCE-1A. EPROM memory starts from address 0000.

6.2.3 SYSTEM DESIGN PARAMETERS

6.2.3.1 Hardware Configuration

The DCE-1 processor module features two powerful LSI subsystems:

- Timer, Interrupt and Communication Control (TICC)
- General Interface Control (GIC)

Complete specifications of the GIC and TICC are given in Sections 2 and 3 of this manual.

The 24 programmable parallel I/O lines are provided by the GIC, and are available at the System Connector. The TICC also provides 8 parallel input lines and 8 parallel output lines. These are available at the Device Connector.

The DCE-1 has a memory-mapped I/O architecture and therefore all the TICC and GIC registers, and the I/O ports can be accessed simply as memory locations. This enables the usage of the powerful memory instruction set of the 8080 CPU, when accessing device registers and I/O ports.

6.2.3.2 Programming Specifications

See Section 5 for full DCE programming specifications.

If the DCE-1 processor module is connected to interface modules via the DCE-BUS, the GIC must be configured in a specific manner. See Section 4 for full details.

The GIC and TICC register addresses are as shown in Table 6-1.

6.2.3.3 Special Considerations

The 8080 CPU requires on Wait state when accessing the slower RAM memory on the earlier DCE-1s. This is automatically taken care of by the logic on the module. RAM memory is usually used for temporary data storage and Stack inmplementation, and therefore these Wait states do not cause any problem at all. However, when attempting to develop and run programs in RAM which utilise one or more TICC interrupts on these earlier versions of DCE-1 there is a possiblity of occasional loss of some interrupts. This is because the TICC interrupt control logic is not ideally suited to taking into account the possible presence of a CPU Wait state when transfering the interrupt RST instruction to the CPU. These earlier versions of DCE-1 can be recognised by the presence of a 74LS02 instead of a 74LS00 on the card.

6.2.3.4 Operational Requirements

Power Requirements

The DCE-1 requires three power supplies: +5V ±5%, -5V ±5%, +12V ±5%. They are usually provided by the DCE-PWR module via the DCE-BUS. Typical power requirements in the quiescent state are given below. Active state values are typically 20% higher.

Number of EPROMs (2708)	+5V	-5V	+12V	unit
0	355	0.1	60	mA
1	355	30	110	mA
2	355	60	160	mA
3	355	90	210	mA
4	355	120	260	mA

Environmental Requirements

Operating temperature : 0°C to 55°C
Storage temperature : -25°C to +85°C
Relative humidity : 95% noncondensing

6.2.4 ORDERING INFORMATION

DCE-1 : Standard Version with 4K EPROM space (4 x 2708)
DCE-1/8S : with socket-mounted 8080
DCE-1A : with 8K EPROM space (4 x 2716)
DCE-1A/8S : with socket-mounted 8080

Serial Interface cables for standard terminals, Utility software package, Assembler/Editor, FORTRAN and BASIC must be ordered separately.

6.3 DCE-2 PROCESSOR MODULES

6.3.1 FEATURES

- complete 8080 microcomputer system on a single 100 x 160 mm eurocard.
- 2K byte RAM and sockets for 4K or 8K byte EPROM.
- opto-isolated serial I/O with programmable Baud rates from 110 to 9600.
- 40 parallel I/O lines; 24 programmable as simple, handshaking or bi-directional with automatic handshake control signals.
- 5 independent interval timers providing 64 microsecond resolution with crystal accuracy.
- 8 independently vectored interrupts.

6.3.2 FUNCTIONAL BLOCK DIAGRAM

Figure 1-2 on page 1-6 shows the general block diagram. Figure 6-1 shows a detailed functional block diagram. RAM memory occupies address space 1000H to 17FFH for DCE-2, and D000H to D7FFH for DCE-2A. EPROM memory starts from ADDRESS 0000.

6.3.3 SYSTEM DESIGN PARAMETERS

6.3.3.1 Hardware Configuration

The DCE-2 processor module features two powerful LSI subsystems:

- Timer, Interrupt and Communication Control (TICC)
- General Interface Control (GIC)

Complete specifications of the GIC and TICC are given in Sections 2 and 3 of this manual.

The 24 programmable parallel I/O lines are provided by the GIC, and are available at the System Connector. The TICC also provides 8 parallel input lines and 8 parallel output lines. These are available at the Device Connector.

The DCE-2 has a memory-mapped I/O architecture and therefore all the TICC and GIC registers, and the I/O ports can be accessed as simple memory locations. This enables the usage of the powerful memory instructions set of the 8080 CPU, when accessing device registers and I/O ports.

The 2K byte RAM memory on the DCE-2 is fast enough for 8080 CPU access without requiring any Wait states.

6.3.3.2 Programming Specifications

See Section 5 for full DCE programming specifications.

If the DCE-2 processor module is connected to interface modules via the DCE-BUS, the GIC must be configured in a specific manner. See Section 4 for full details.

The GIC and TICC register addresses are as shown in Table 6-1.

6.3.3.3 Operational Requirements

Power Requirements

The DCE-2 requires three power supplies: +5V ±5%, -5V ±5%, +12V ±5%. They are usually provided by the DCE-PWR module via the DCE-BUS. Typical power requirements in the quiescent state are given below. Active state values are typically 20% higher.

Number of EPROMs (2708)	+5V	-5V	+12V	unit
0	460	0.1	70	mA
1	460	30	120	mA
2	460	60	170	mA
3	460	90	220	mA
4	460	120	270	mA

Environmental Requirements

Operating temperature : 0°C to 55°C
Storage temperature : -25°C to +85°C
Relative humidity : 95% noncondensing

6.3.4 ORDERING INFORMATION

DCE-2 : Standard Version with 4K EPROM space (4 x 2708)
DCE-2/8S : with socket-mounted 8080
DCE-2A : with 8K EPROM space (4 x 2716)
DCE-2A/8S : with socket-mounted 8080

Serial interface cables for standard terminals, Utility software package, Assembler/Editor, FORTRAN and BASIC must be ordered separately.

6.4 DCE-X PROCESSOR MODULE

6.4.1 FEATURES

- memory expandable 8080 microcomputer system on a single 100 x 160 mm eurocard.
- hardware, software and pin compatible with DCE-1A and DCE-2A microcomputers.
- memory expandable up to 64K bytes with MX PROM and/or RAM memory modules.
- flat-cable X-BUS connection to support 1 to 8 memory modules.
- opto-isolated serial I/O with programmable Baud rates from 110 to 9600.
- 40 parallel I/O lines; 24 programmable as simple, handshaking, or bidirectional, with automatic handshake control signals.
- 5 independent internal timers providing 64 microsecond resolution with crystal accuracy.
- 8 independently vectored interrupts.

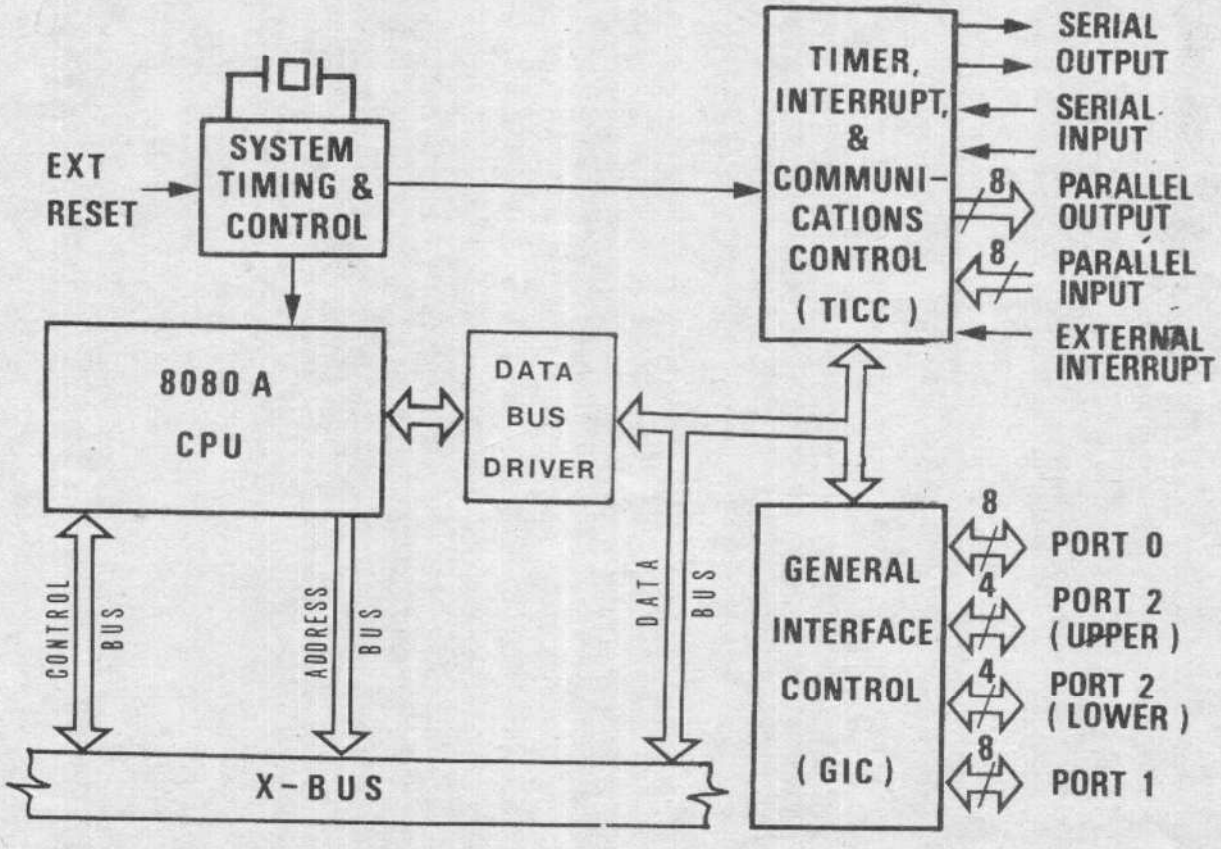


Figure 6-3 : Functional Block Diagram

6.4.2 FUNCTIONAL BLOCK DIAGRAM

Figure 6-3 shows the functional block diagram. The detailed block diagram of Figure 6-1 applies also to the DCE-X, except for the absence of memory on the DCE-X module.

6.4.3 SYSTEM DESIGN PARAMETERS

6.4.3.1 Hardware Configuration

The DCE-X is functionally equivalent to and plug compatible with DCE-1A and DCE-2A processor modules. All DCE-1A, DCE-2A documentation and specifications apply to the DCE-X with the exception of the resident memory on the module.

The DCE-X forms the base of the memory-expandable DCE series, with up to 64K bytes of PROM and RAM memory in any combination. A flat-cable X-BUS connector allows the DCE-X to be linked with up to eight MX memory modules in any combination, to provide up to a maximum of 64K bytes of memory. No memory is provided on the DCE-X. Standard X-BUS cables are available for connecting memory modules. All X-BUS signals are buffered. The cables are kept short with critical signals screened, to eliminate noise problems.

6.4.3.2 Programming Specifications

The TICC and GIC register addresses for the DCE-X are different from those given in Figure 6-2. These register address differences between the different DCE processor modules are automatically resolved by the resident Assembler in the DCE-DM development system, when translating TICC and GIC macros. Table 6-1 shows the TICC and GIC register addressing for the DCE-X.

The DCE-X address space is organised to allow optimum usage of external memory. A summary of DCE-X address space is given below:

ADDRESS (HEX)	ALLOCATION
0000 - FEFF	External Memory
FF00 - FF03	GIC Register and Ports
FF08	GIC Port 0 with synchronised I/O
FF10 - FF1D	TICC Registers, Ports and Timers

For GIC and TICC addressing, address bits 5,6,7 are don't care states.

6.4.3.3 X-BUS Signal Allocation

The DCE user need not normally be concerned with the X-BUS characteristics. This information is provided only for those users who intend designing their own X-BUS compatible modules.

PIN NUMBER	MNEMONIC	DESCRIPTION
1	GROUND	screening line
2	D0	data bit 0
3	GROUND	screening line
4	D1	data bit 1
5	GROUND	screening line
6	D2	data bit 2
7	GROUND	screening line
8	D3	data bit 3
9	GROUND	screening line
10	D4	data bit 4
11	GROUND	screening line
12	D5	data bit 5
13	GROUND	screening line
14	D6	data bit 6
15	GROUND	screening line
16	D7	data bit 7
17	GROUND	screening line
18	—	no connection
19	GROUND	screening line
20	MEMW	memory Write strobe
21	GROUND	screening line
22	DBIN	CPU input strobe
23	A10	address line 10
24	$\overline{\text{MEMR}}$	memory Read strobe
25	A14	address line 14
26	A11	address line 11
27	A12	address line 12
28	A13	address line 13
29	A9	address line 9
30	A15	address line 15
31	A7	address line 7
32	A8	address line 8
33	A5	address line 5
34	A6	address line 6
35	A3	address line 3
36	A4	address line 4
37	A1	address line 1
38	A2	address line 2
39	A0	address line 0
40	INTA	interrupt acknowledge
41	GROUND	screening line
42	$\overline{\text{WRQ}}$	Wait cycle request
43	WAIT	CPU Wait acknowledge
44	INTE	CPU interrupt enable
45	GROUND	screening line
46	$\overline{\text{HOLDA}}$	CPU Hold acknowledge
47	$\overline{\text{INT}}$	interrupt request
→ 48	CK2(TTL)	TTL level clock (2 MHz)
49	$\overline{\text{HOLD}}$	Hold request
50	SYNC	CPU SYNC signal

6.4.3.4 X-BUS Electrical Specifications

SIGNAL	MIN.	TYP.	MAX.	CONDITIONS
ADDRESS, INTE	3.7V		0,45V	1.9 mA -150µA
DATA OUTPUT	3.65V	0.3V 4.0V	0.45V	15mA -1mA
DATA INPUT	2.0V		0.95V	
DATA IN leakage				60µA
MEMW, $\overline{\text{MEMR}}$, INTA	2.7V	0.35V 3.4V	0.5V	8mA -400µA
$\overline{\text{HOLD}}$	2.7V		0.4V	-1.2mA 0.25mA
$\overline{\text{HOLDA}}$	2.4V	0.26V 3.4V	0.4V	48mA -1.2mA
WAIT	3.3V		0.4V	-0.4mA
DBIN	3.7V		0.45V	1.1mA -190µA
CK2	2.4V		0.45V	15mA -1mA
SYNC	3.7V		0.45V	1.65mA -150µA
$\overline{\text{WRQ}}$	2.7V		0.4V	-0.8mA 0.25mA
$\overline{\text{INT}}$	2.4V		0.4V	-1.6mA 40µA

6.4.3.5 X-BUS Timing (relative to the 8080 CPU)

SIGNAL	TYP.	MAX.	CONDITIONS
DATA OUT	15ns	25ns	after 8080 output
DATA IN	20ns	30ns	before 8080 input
$\overline{\text{MEMR}}$, MEMW	10ns	20ns	relative to DBIN
$\overline{\text{HOLD}}$, $\overline{\text{HOLDA}}$	14ns	22ns	relative to 8080

6.4.3.6 Operational Requirements

Power requirements

The DCE-X requires three power supplies. These are usually provided by the DCE-PWR module via the DCE-BUS. Typical power requirements in the quiescent state are given below. Active state values are typically 20% higher.

+12V $\pm$ 5% : 70mA
+5V $\pm$ 5% : 375mA
-5V $\pm$ 5% : 0.1mA

Environmental Requirements

Operating temperature : 0°C to 55°C
Storage temperature : -25°C to +85°C
Relative humidity : 95% noncondensing

6.4.4 ORDERING INFORMATION

DCE-X : Standard Version

DCE-X/8S : with socket mounted 8080

X-BUS(n) : flat-cable bus connection between DCE-X and 'n' (n = 1 to 8) memory modules.
- must be ordered separately.

Interface cables for standard terminals, Utility software package, Assembler/Editor, FORTRAN and BASIC must be ordered separately.

6.5 MX-84 : COMBINATION MEMORY EXPANSION MODULE

6.5.1 FUNCTIONAL DESCRIPTION

The MX-84 module provides 8K bytes of PROM space and 4K bytes of static RAM as expansion memory for DCE-X processor based systems.

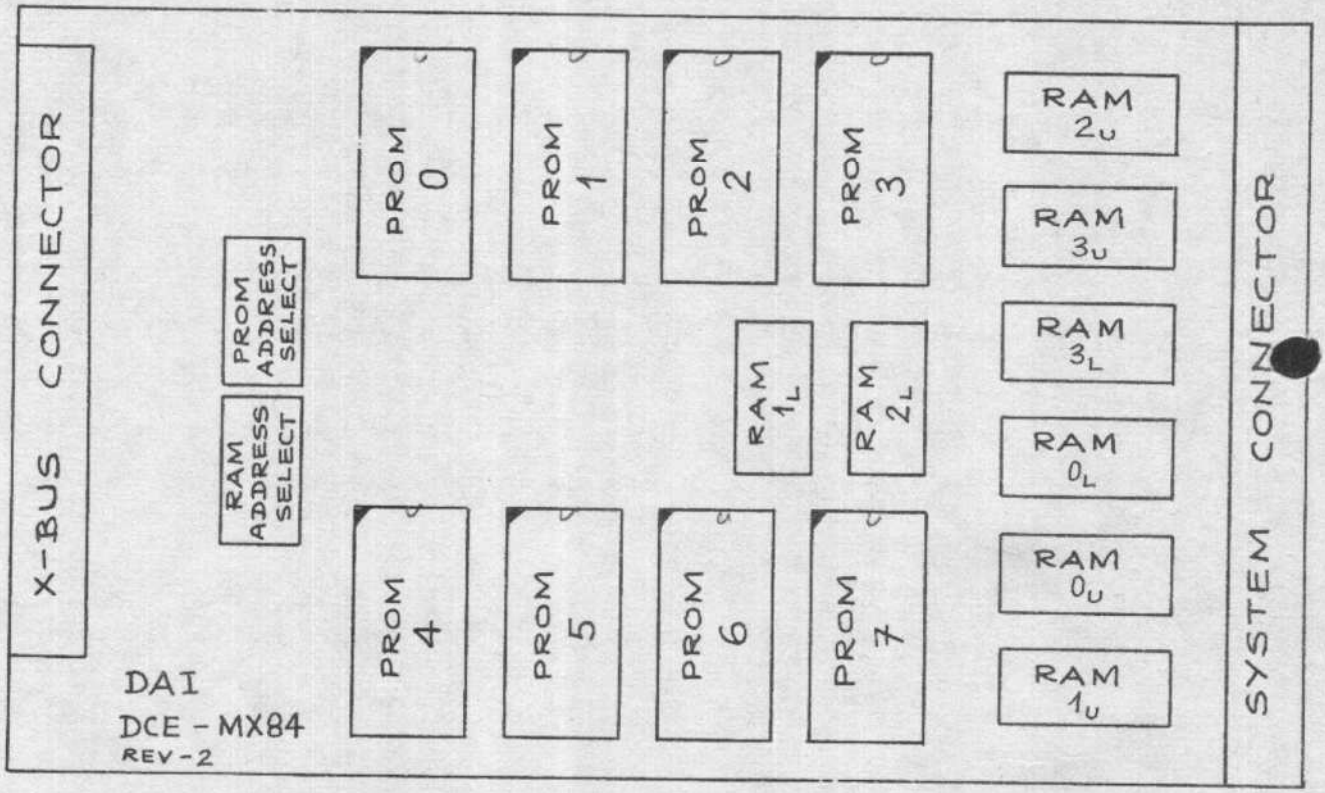
Up to eight 2708 or equivalent PROM/ROM devices can be inserted into the sockets provided. The PROM/ROM and RAM access times allow the 8080 CPU on the DCE-X to run at full speed. Two address select switches on the module allow the PROM and RAM memories to occupy any desired ranges in DCE-X memory address space.

One or more MX-84 modules, along with other MX memory modules, can be easily connected to a DCE-X processor via the flat-cable X-BUS connector.

6.5.2 FEATURES

- 8K byte PROM space and 4K byte fast RAM
- runs at full 8080 CPU speed (? 2MHz)
- switch selectable PROM memory base address
- switch selectable RAM memory base address
- X-BUS connection to DCE-X processor module
- single 100 x 160 mm eurocard format.

6.5.3 MODULE LAYOUT



6.5.4 ADDRESS SELECTION

The PROM and RAM base addresses can be separately selected using the two hexadecimal rotary switches located near the X-BUS connector on the module.

The upper switch, when the module is held with its name in the bottom left corner, controls the PROM addresses in steps of 8K bytes. The lower switch controls the RAM addresses in steps of 4K bytes.

PROM Base Address Selection

Each PROM socket on the MX-84 module is associated with a unique 1K address block relative to the selected PROM base address. The physical positions of the PROM sockets are as shown in the module layout diagram. PROM 0 occupies the lowest address range. All PROM sockets indicate the correct insertion orientation by a rounded internal corner at pin 1.

The PROM base address may be set to any 8K byte boundary as shown below:

Upper Switch Setting	PROM Start Address (Hex)	PROM End Address (Hex)
0	0000	1FFF
1	2000	3FFF
2	4000	5FFF
3	6000	7FFF
4	8000	9FFF
5	A000	BFFF
6	C000	DFFF
7*	E000	FFFF

PSG DAI: 0 → 1-8

1 9-16

* When using this range do not insert PROM 7, since it will conflict with addressing for the GIC and TICC registers on the DCE-X module.

RAM Base Address Selection

The MX-84 module has 4K bytes of fast static RAM, occupying a 4K address block relative to the RAM base address.

The RAM base address may be set to any 4K byte boundary as shown below:

Lower Switch Setting	RAM Start Address (Hex)	RAM End Address (Hex)
0	0000	0FFF
1	1000	1FFF
2	2000	2FFF
3	3000	3FFF
4	4000	4FFF
5	5000	5FFF
6	6000	6FFF
7	7000	7FFF
8	8000	8FFF
9	9000	9FFF
A	A000	AFFF
B	B000	BFFF
C	C000	CFFF
D	D000	DFFF
E	E000	EFFF
F*	F000	FFFF

* This setting should not be used due to the conflict with DCE-X GIC and TICC register addressing.

P60 : 0 - 3FFF → ROM

B000 - CFFF → RAM

6.5.5 OPERATIONAL REQUIREMENTS

Power Requirements

The MX-84 module requires three power supplies. These are obtained from the DCE-BUS via the System Connector. The module is not connected to any other signal on the DCE-BUS.

Typical power requirements in the quiescent state, without any PROMs, are given below. Active state values are typically 20% higher.

+5V : 600mA
-5V : 0
+12V : 0

Environmental Requirements

Operating temperature : 0°C to 55°C
Storage temperature : -25°C to +85°C
Relative humidity : up to 95% noncondensing

X-BUS Loading

SIGNAL	LEAKAGE	DRIVE (RAM)	LOAD (RAM)
Address Lines Data Lines Read, Write	one CMOS 80µA max.	2.1mA @ 0.4V -1mA @ 2.4V	one CMOS 80µA max. -360µA @ 0.4V

6.5.6 ORDERING INFORMATION

MX-84 : Standard Version, supplied without PROMs

The X-BUS(n) cable for connection between DCE-X and 'n' (1 to 8) memory modules must be ordered separately.

6.6 MXP-12 : 12K PROM MEMORY EXPANSION MODULE

6.6.1 FUNCTIONAL DESCRIPTION

The MXP-12 module provides 12K bytes of PROM space as expansion memory for DCE-X processor based systems. Up to twelve 2708 or equivalent PROM/RAM devices can be inserted into the sockets provided, and they allow the 8080 CPU on the DCE-X to run at full speed.

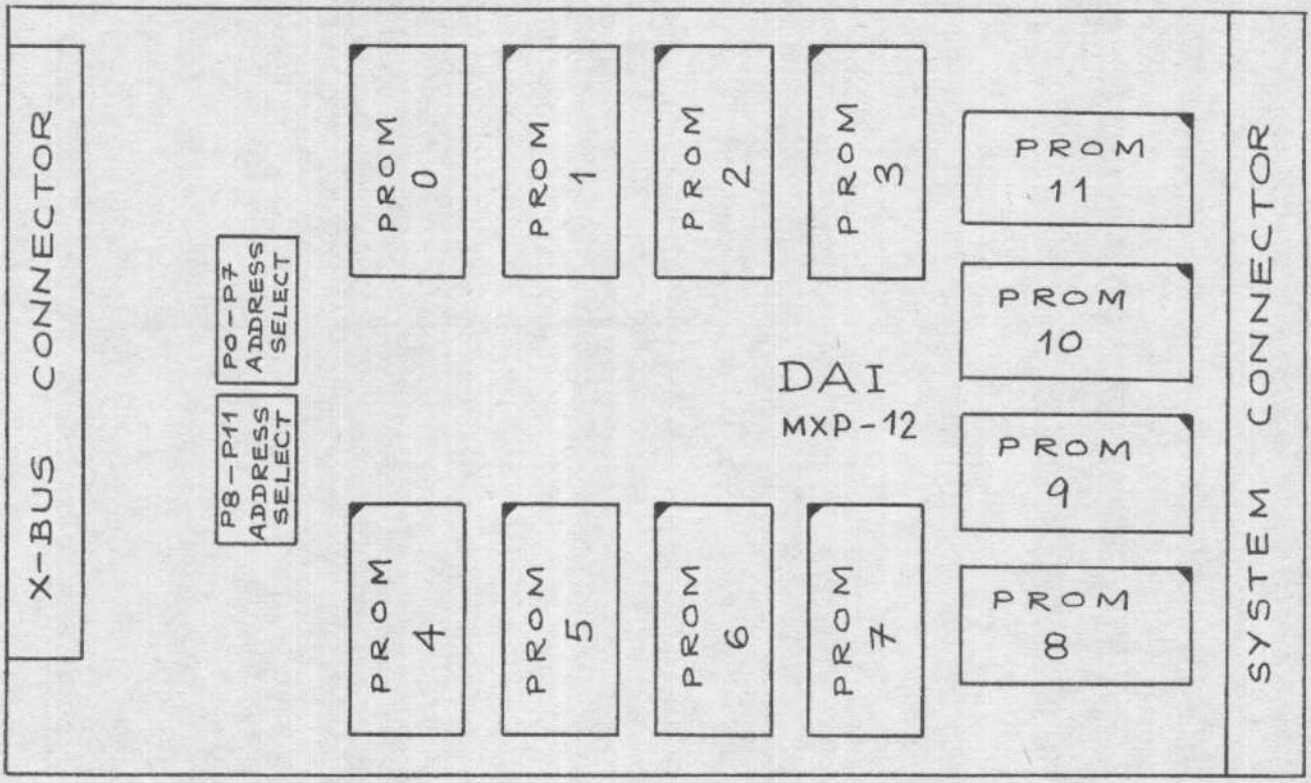
The memory space on the MXP-12 is organised into two banks of 4K and 8K bytes. Each bank can be assigned a separate base address by means of two rotary switches.

One or more MXP-12 modules, along with other MX memory modules, can be easily connected to a DCE-X processor via the flat-cable X-BUS connector.

6.6.2 FEATURES

- 12K PROM space, organised into two banks of 4K and 8K bytes
- separate switch selectable base addresses for the two memory banks
- runs at full 8080 CPU speed
- X-BUS connection to DCE-X processor module
- single 100 x 160 mm eurocard format.

6.6.3 MODULE LAYOUT



6.6.4 ADDRESS SELECTION

Each PROM socket on the MXP-12 module is associated with a unique 1K address block. PROMs 0 to 7 constitute the 8K bank, and PROMs 8 to 11 constitute the 4K bank. The physical positions of the PROM sockets are shown in the module layout diagram. PROMs 0 and 8 occupy the lowest address ranges in the two banks. All PROM sockets indicate the correct insertion orientation by a rounded internal corner at pin 1.

The base address for the 4K and 8K banks can be separately selected using the two hexadecimal rotary switches located near the X-BUS connector on the module.

The switch at the top, when the module is held so that the name can be correctly read, controls the base address of the 8K bank (PROM 0 to 7) in steps of 8K. The lower switch controls the base address of the 4K bank (PROM 8 to 11) in steps of 4K.

8K Memory Base Address Selection

The base address may be set to any 8K byte boundary as shown below:

Upper Switch Setting	8K Bank Start Address (Hex)	8K Bank End Address (Hex)
0	0000	1FFF
1	2000	3FFF
2	4000	5FFF
3	6000	7FFF
4	8000	9FFF
5	A000	BFFF
6	C000	DFFF
7*	E000	FFFF

* When using this range do not insert PROM 7, since it will conflict with addressing for the GIC and TICC registers on the DCE-X module.

4K Memory Base Address Selection

The base address may be set to any 4K byte boundary as shown below:

Lower Switch Setting	4K Bank Start Address (Hex)	4K Bank End Address (Hex)
0	0000	0FFF
1	1000	1FFF
2	2000	2FFF
3	3000	3FFF
4	4000	4FFF
5	5000	5FFF
6	6000	6FFF
7	7000	7FFF
8	8000	8FFF
9	9000	9FFF
A	A000	AFFF
B	B000	BFFF
C	C000	CFFF
D	D000	DFFF
E	E000	EFFF
F*	F000	FFFF

* When using this range do not insert PROM 11, since it will conflict with addressing for the GIC and TICC registers on the DCE-X module.

6.6.5 OPERATIONAL REQUIREMENTS

Power Requirements

The MXP-12 module requires three power supplies. These are obtained from the DCE-BUS via the System Connector. No other DCE-BUS signals are connected to this module.

Typical power requirements in the quiescent state, without any PROMs, are given below. Active state values are typically 20% higher.

+5V	:	100mA
-5V	:	0
+12V	:	0

Environmental Requirements

Operating temperature	:	0°C to 55°C
Storage temperature	:	-25°C to +85°C
Relative humidity	:	up to 95% noncondensing

X-BUS Loading

This depends on the PROMs used.

6.6.6 ORDERING INFORMATION

MXP-12 : Standard Version, supplied without PROMs.

The X-BUS(n) cable for connection between DCE-X and 'n' (1 to 8) memory modules must be ordered separately.

6.7 MXR-8 : 8K RAM MEMORY EXPANSION MODULE

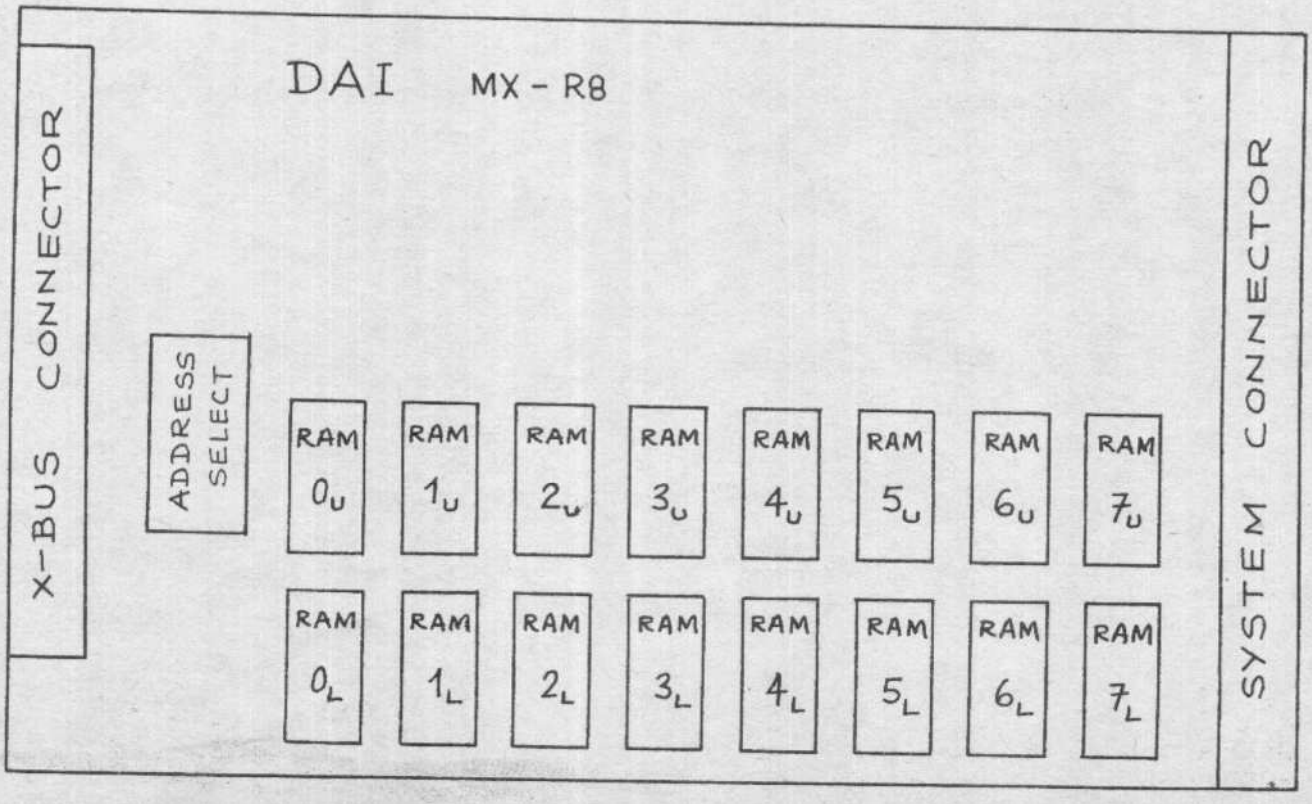
6.7.1 FUNCTIONAL DESCRIPTION

The MXR-8 module provides 8K bytes of static RAM as expansion memory for DCE-X processor based systems. The RAM on the module is fast enough to allow the 8080 CPU on the DCE-X to run at full speed. An address select switch allows the RAM to occupy any desired range in DCE-X memory address space. One or more MXR-8 modules, along with other MX memory modules, can be easily connected to a DCE-X processor via the flat-cable X-BUS connector.

6.7.2 FEATURES

- 8K byte RAM memory
- runs at full 8080 CPU speed
- switch selectable RAM base address
- X-BUS connection to DCE-X processor module
- single 100 x 160 mm eurocard format.

6.7.3 MODULE LAYOUT



6.7.4 ADDRESS SELECTION

The RAM memory base address can be selected using the hexadecimal rotary switch located near the X-BUS connector on the module.

The RAM base address may be set to any 8K byte boundary as shown below:

Switch Setting	RAM Start Address (Hex)	RAM End Address (Hex)
0	0000	1FFF
1	2000	3FFF
2	4000	5FFF
3	6000	7FFF
4	8000	9FFF
5	A000	BFFF
6	C000	DFFF
7*	E000	FFFF

* This setting should not be used due to the conflict with DCE-X GIC and TICC register addressing.

6.7.5 OPERATIONAL REQUIREMENTS

Power Requirements

The MXR-8 module requires a single +5V power supply. This is obtained from the DCE-BUS via the System Connector. No other DCE-BUS signals are connected to the module.

A typical power requirement in the quiescent state is given below. Active state value is typically 20% higher.

+5V : 1.2A

Environmental Requirements

Operating temperature : 0°C to 55°C
Storage temperature : -25°C to +85°C
Relative humidity : up to 95% noncondensing

X-BUS Loading

SIGNAL	LEAKAGE	DRIVE	LOAD
Address Lines	one CMOS		one CMOS
Data Lines	160µA max.	2.1mA @ 0.4V -1mA @ 2.4V	160µA max.
Read, Write			-360µA @ 0.4V

6.7.6 ORDERING INFORMATION

MXR-8 : Standard Version

The X-BUS(n) cable for connection between DCE-X and 'n' (1 to 8) memory modules must be ordered separately.

6.8 MXR-4 : 4K RAM MEMORY EXPANSION MODULE

6.8.1 FUNCTIONAL DESCRIPTION

The MXR-4 module economically provides 4K bytes of static RAM as expansion data memory for DCE-X processor based systems. The 8080 CPU on the DCE-X requires one Wait state when accessing the slower RAM memory on the MXR-4. This is automatically taken care of by the logic on the module.

An address select switch allows the RAM to occupy any desired range in DCE-X memory address space. One or more MXR-4 modules, along with other MX memory modules, can be easily connected to a DCE-X processor via the flat-cable X-BUS connector.

6.8.2 FEATURES

- 4K byte slow RAM memory
- switch selectable RAM base address
- X-BUS connection to DCE-X processor module
- single 100 x 160 mm eurocard format.

6.8.3 ADDRESS SELECTION

The RAM memory base address can be selected using the hexadecimal rotary switch located near the X-BUS connector on the module.

The RAM base address may be set to any 4K byte boundary as shown below:

Address Switch Setting	RAM Start Address (Hex)	RAM End Address (Hex)
0	0000	0FFF
1	1000	1FFF
2	2000	2FFF
3	3000	3FFF
4	4000	4FFF
5	5000	5FFF
6	6000	6FFF
7	7000	7FFF
8	8000	8FFF
9	9000	9FFF
A	A000	AFFF
B	B000	BFFF
C	C000	CFFF
D	D000	DFFF
E	E000	EFFF
F*	F000	FFFF

* This setting should not be used due to the conflict with DCE-X GIC and TICC register addressing.

6.8.4 SPECIAL CONSIDERATIONS

The 8080 CPU on the DCE-X requires one Wait state when accessing the slower RAM memory provided on the earlier MX-4s. This is automatically taken care of by the logic on the MXR-4 module. When this RAM memory is used for temporary data storage and Stack implementation, the Wait state does not cause any problems at all.

When attempting to run programs in RAM which utilize one or more TICC interrupts, there is a possibility of occasional loss or misinterpretation of interrupts. This is because the TICC interrupt control logic is not ideally suited to taking into account the possible presence of a CPU Wait state, when transferring the interrupt RST instruction to the CPU on the DCE-X.

6.8.5 OPERATIONAL REQUIREMENTS

Power Requirements

The MXR-4 module requires a single +5V power supply. This is obtained from the DCE-BUS via the System Connector. No other DCE-BUS signals are connected to the module.

A typical power requirement in the quiescent state is given below. Active state value is typically 20% higher.

+5V : 1.2A

Environmental Requirements

Operating temperature	:	0°C to 55°C
Storage temperature	:	-25°C to +85°C
Relative humidity	:	up to 95% noncondensing

X-BUS Loading

SIGNAL	LEAKAGE	DRIVE	LOAD
Address Lines	one CMOS		one CMOS
Data Lines	320µA	2ma @ 0.45V -200µA @ 2.4V	320µA
Read, Write			-360µA @ 0.4V

6.8.6 ORDERING INFORMATION

MXR-4 : Standard Version

The X-BUS(n) cable for connection between DCE-X and 'n' (1 to 8) memory modules must be ordered separately.

6.9 DCE-LSA : LARGE SYSTEM ADAPTER MODULE

Preliminary Specification

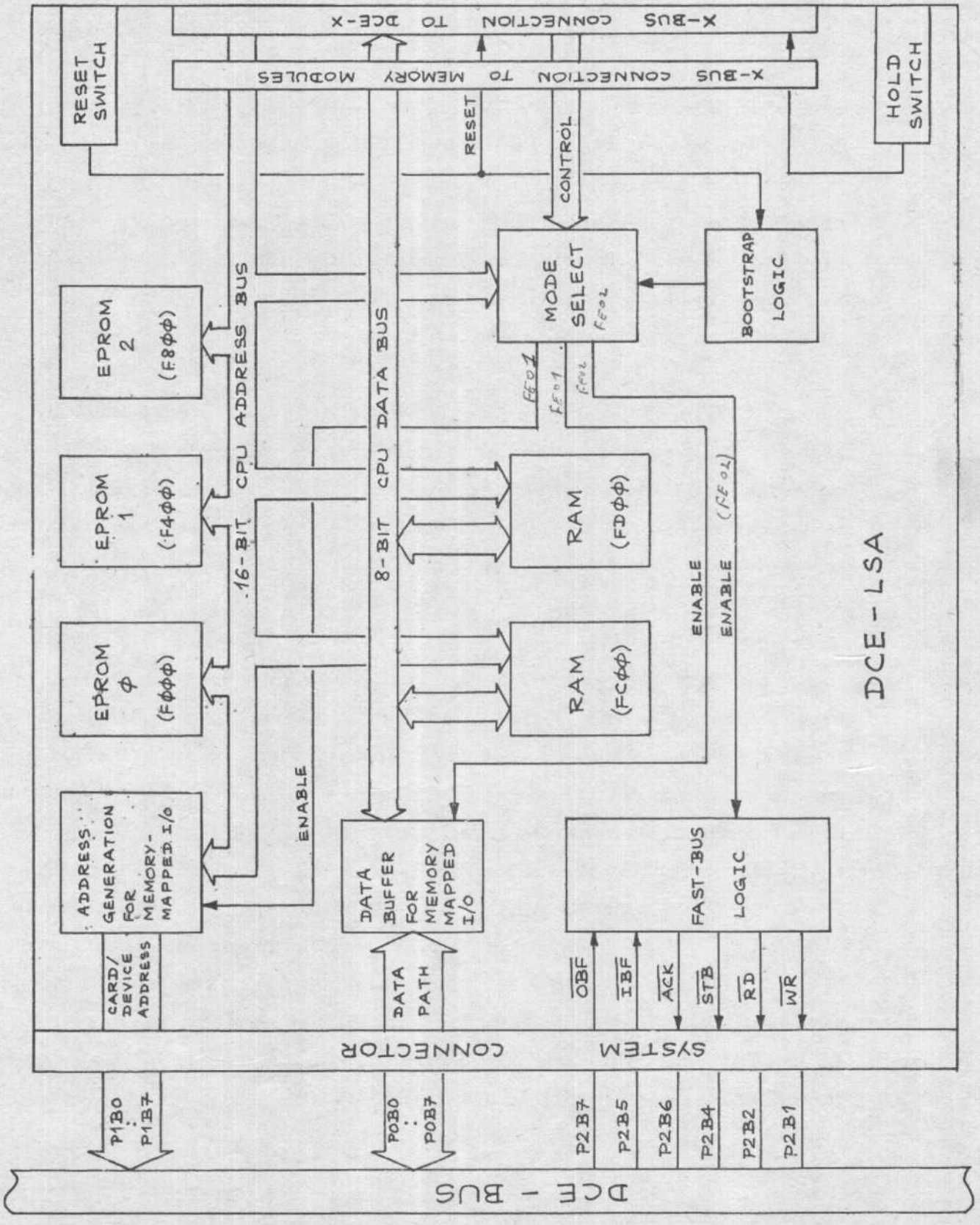
6.9.1 FUNCTIONAL DESCRIPTION

The DCE-LSA module enables the realisation of fast high-performance systems using the DCE-X microcomputer module. It is ideally suited for realising large systems based on the DCE-X microcomputer for optimum speed characteristics. It can provide a memory-mapped I/O architecture for DCE-BUS compatible modules to reduce the access time to two machine cycles of the DCE-X CPU. 512 bytes of RAM and sockets for 3K bytes EPROM in high address space are provided on the DCE-LSA module for housing the Utility or equivalent, and for work areas. This leaves the full capacity on added DCE-X memory expansion modules free for the user. A Reset button and an automatic bootstrap feature transfer control to the Utility program or equivalent residing on the card, in high address space, automatically on reset. This leaves lower address space starting from 0000H free for the user. A Hold switch enables the DCE-X CPU to be stopped and started at any time without loss of status. The DCE-LSA module can also be software configured for implementing the DCE Fast-Bus (see Section 4.1.4), or the normal DCE-BUS.

6.9.2 FEATURES

- reset button and bootstrap feature for automatic transfer of control to resident software in high address space on reset
- frees lower address space starting from 0000H for the user
- provides memory-mapped architecture, DCE Fast-Bus or normal DCE-BUS for accessing DCE-BUS compatible modules
- implements the DCE Fast-Bus by generating the necessary control signals automatically
- 512 bytes of RAM and sockets for 3K bytes EPROM in high address space, for the Utility program or equivalent and work areas
- full capacity on added memory expansion modules free for the user
- hold switch for stopping and starting the DCE-X CPU at will

6.9.3 MODULE LAYOUT AND BLOCK DIAGRAM



6.9.4 SYSTEM DESIGN PARAMETERS

6.9.4.1 Hardware Configuration

The DCE-LSA module has 2 flat-cable X-BUS connectors, for use in DCE-X based systems. The connector located at the edge of the module is for connection to the DCE-X processor module via an X-BUS (1) cable. The other is used for connecting DCE-X memory expansion modules via the X-BUS (n) cable (n = 1 to 8). The DCE-LSA thus acts as an intermediate stage between the DCE-X, and the memory and DCE-BUS compatible interface modules.

The DCE-LSA can be used to implement a memory-mapped I/O architecture, DCE Fast-Bus (see Section 4.1.4), or normal DCE-BUS for accessing DCE-BUS compatible modules. One of these three modes is selected when the DCE-X CPU performs a Write operation (data is irrelevent) to address locations 0FE01H, 0FE02H or 0FE03H respectively.

In the memory-mapped I/O mode, the DCE-LSA drives the DCE-BUS directly from the DCE-X CPU signals, and therefore the GIC ports on the DCE-X must be configured in the input mode to avoid conflicts. In this mode the registers and data devices on the DCE-BUS compatible modules appear as memory locations to the CPU on the DCE-X. The DCE-LSA generates the DCE-BUS $\overline{RD}$ and $\overline{WR}$ signals from the CPU Read and Write control signals, when the CPU address lines contain 0FE00H to 0FEFFH. When the 8 high-order address lines contain 0FEH, the 8 low-order address lines are gated onto the card/device address lines of the DCE-BUS, and the bi-directional drivers on the DCE-LSA between the DCE-BUS data path and CPU data bus are driven in accordance with the $\overline{RD}$ and $\overline{WR}$ signal status.

In the Fast-Bus mode the DCE-LSA does not drive the DCE-BUS, and instead the DCE-X GIC is configured in bi-directional mode for driving the DCE-BUS (see Section 4.1.4).

In the normal DCE-BUS mode the DCE-X GIC drives the DCE-BUS just as in non DCE-LSA systems.

The DCE-LSA has 512 bytes of RAM and sockets for 3K bytes EPROM in high address space. The Reset button on the DCE-LSA is used as a system reset and to transfer control to the start of the EPROM space on the module. The reset activates a logic unit on the DCE-LSA, which inverts CPU address lines A15, A14, A13, A12, thus producing an effective address of 0F000H instead of 0000H. This is the start address of EPROM space on the DCE-LSA. A suitable program (eg: the Utility) at this location can then take over control, and perform necessary functions. The address inversion logic remains active until address line A15 goes high. By placing the instruction 'JMP 0F003H' or similar at address 0F000H it is possible to make address line A15 go high and disable the 4 address inverters. They will remain disabled until the reset button on the DCE-LSA is pushed again. This scheme acts as an automatic bootstrap procedure, while leaving the lower address space (including address 0000H) completely free for the user.

6.9.4.2 Programming Specifications

Initialisation

The first instruction located at the beginning of PROM space on the DCE-LSA module (at start address 0F000H) should be 'JMP 0F003H' in order to reset the bootstrap logic as explained earlier.

After power-on or system reset, the DCE-LSA must be initialised to select one of the three possible DCE-BUS operation modes. This is done simply by performing a DCE-X CPU write operation (data is irrelevent) to one of three special address locations :

0FE01H : memory-mapped I/O mode
(DCE-LSA drives DCE-BUS)

0FE02H : Fast-Bus mode
(DCE-X GIC drives DCE-BUS)

0FE03H : normal DCE-BUS mode
(DCE-X GIC drives DCE-BUS)

For example, the Fast-Bus mode can be selected simply by a STA 0FE02H' instruction (contents of Accumulator are irrelevant).

Before selecting the memory-mapped I/O mode, ensure that the DCE-X GIC is configured in the input mode to avoid conflicts and possible damage to the GIC. The GIC will automatically be in the input mode after a power-on or system reset.

DCE-LSA Memory Addressing

The 512 bytes of RAM and sockets for 3K EPROM occupy high address space :

0F000H - 0FBFFH : 3K byte EPROM memory on DCE-LSA
0FC00H - 0FDFFH : 512 byte RAM memory on DCE-LSA

Memory-Mapped I/O Mode Addressing

In memory-mapped I/O mode the following addressing scheme is used:

0FE10H - 0FEFFH : read and write operations to DCE-BUS compatible interface modules

When used with DAI 'Real-World' interface modules (RWC-), the low-order 8 bits of the above address are decoded as follows :

Bits 4-7 : module select (1 to 15, corresponding to module address select switch setting in the range 1 to F).

Bits 0-3 : register select within the selected module.

For example, RIC Port 1 of a RWC module with address select switch set to A (Hex) can be read into the DCE-X CPU Accumulator by the single instruction :

```
LDA     0FEA1H
```

Similarly, all the RIC ports of a RWC module with address select switch set to B (Hex) can be configured as output as follows :

```
MVI     A,80H     ;set up control word
STA     0FEB3H    ;write to RIC command register
```

It is also possible for example, to set up a counter directly at one of the RIC Ports configured as output on a RWC module.

DCE Utility Software

Three different versions of the Utility program are available corresponding to the three modes of DCE-BUS operation :

UPT	LS.nn	:	3K Utility for DCE-LSA, standard DCE-BUS
UPT	LF.nn	:	3K Utility for DCE-LSA, Fast-Bus
UPT	LM.nn	:	3K Utility for DCE-LSA, Memory-mapped I/O

(nn = baud rate code)

6.9.4.3 Module Connector Definitions

System Connector

See Section 6.1.4 for the pin definitions.

X-BUS Connectors

See Section 6.4.3.3 for the pin definitions of both these connectors.

6.9.4.4 Operational Requirements

Power Requirements

The DCE-LSA requires three power supplies from the DCE-BUS. The values given below are for the quiescent state with the three 2708 EPROMs plugged in. Active state values are typically 20% higher.

+12V $\pm$5%	:	80 mA
+ 5V $\pm$5%	:	380 mA
- 5V $\pm$5%	:	52 mA

Environmental Requirements

Operating temperature	:	0°C to 55°C
Storage temperature	:	-25°C to +85°C
Relative humidity	:	95% noncondensing

6.9.5 ORDERING INFORMATION

DCE-LSA	:	Standard version
X-BUS(1)	:	Flat-cable for connecting to DCE-X - must be ordered separately
X-BUS(n)	:	Flat-cable connecting upto 'n' DCE-X memory expansion modules - must be ordered separately

6.9.6 DCE-LSA APPLICATION EXAMPLE: INTEL MDS EMULATOR

The DCE-LSA card with a suitable DCE-X based configuration can emulate the entire functions of the paper-tape oriented INTEL MDS Development System. A DCE configuration for this requires a paper-tape reader, paper-tape punch, a printer and a console device as peripherals. The DCE-LSA Utility program contains all of the normal DCE Utility functions, together with peripheral driver routines. The DCE based MDS emulator allows development software such as Assembler and Editor to reside permanently in EPROM. This eliminates the need to load the Assembler and Editor from paper-tape each time they are needed.

The minimum configuration is given below.

1	RACK-I
2	DCE-PWR/H heavy duty power supply
1	DCE-X
1	DCE-LSA
1	X-BUS(3)
1	MXR-8 (adr. switch = 0)
1	MXR-8 (adr. switch = 1)
1	MXP-12 (adr. switches : top = 6, bottom = B)
2	RWC-T24
1	3K Utility program for DCE-LSA

The 2 RWC-T24 modules provide the handshake interfaces for the printer, paper-tape reader and punch. Driver software is included in the DCE-LSA Utility.

Address Space

0000 -	all available RAM
B000 - E3FF	PROM copy of MDS Editor and Assembler
F000 - FBFF	3K byte DCE-LSA Utility, MDS transfer vectors + I/O drivers.
FC00 - FDFF	512 byte RAM on DCE-LSA
FE00 - FEFF	DCE-LSA address space for DCE-BUS compatible module interfacing.
FF00 - FFFF	DCE-X GIC and TICC addresses

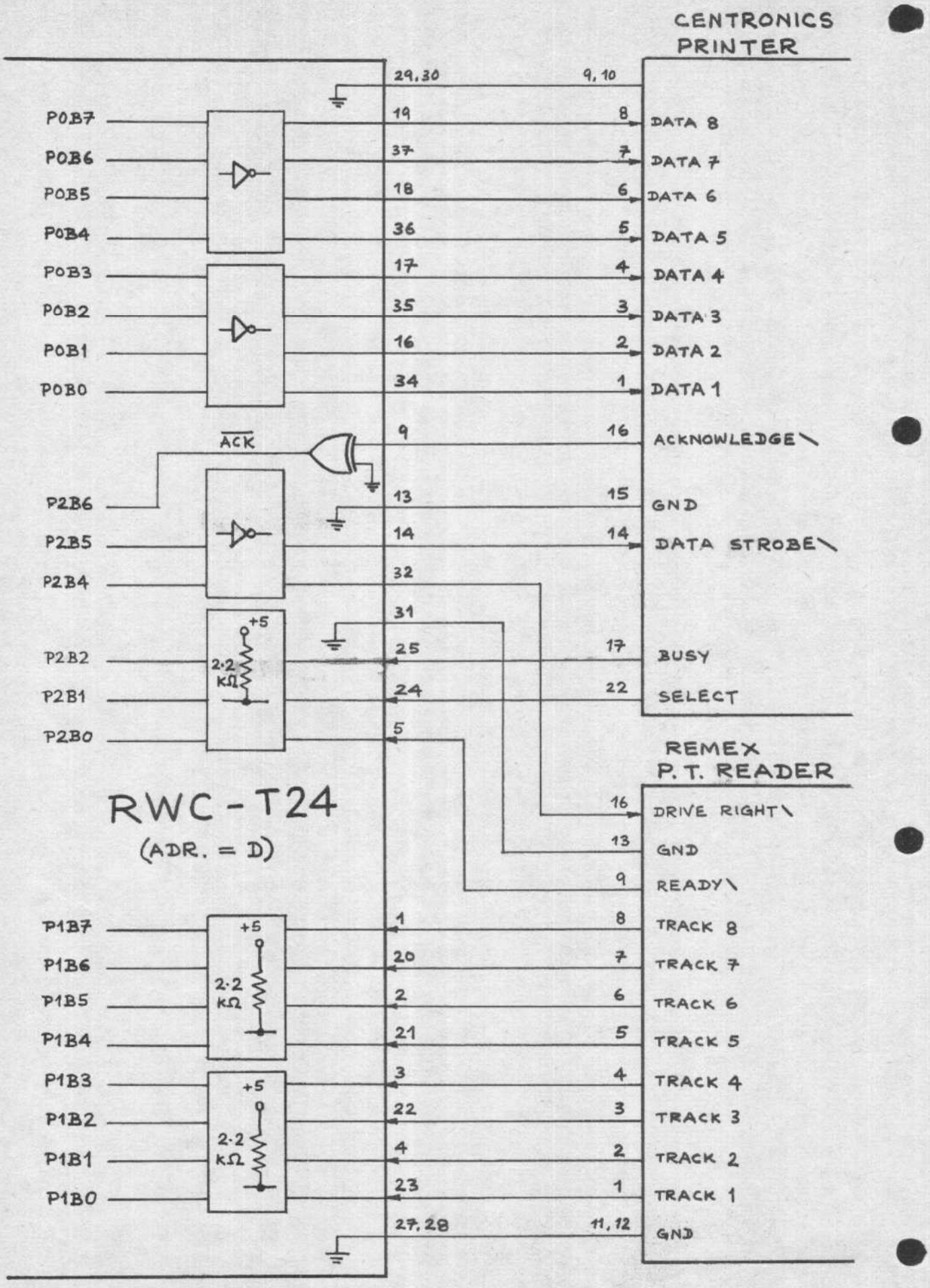


Figure 6-4 : RWC-T24 Interface to Printer and Paper-Tape Reader

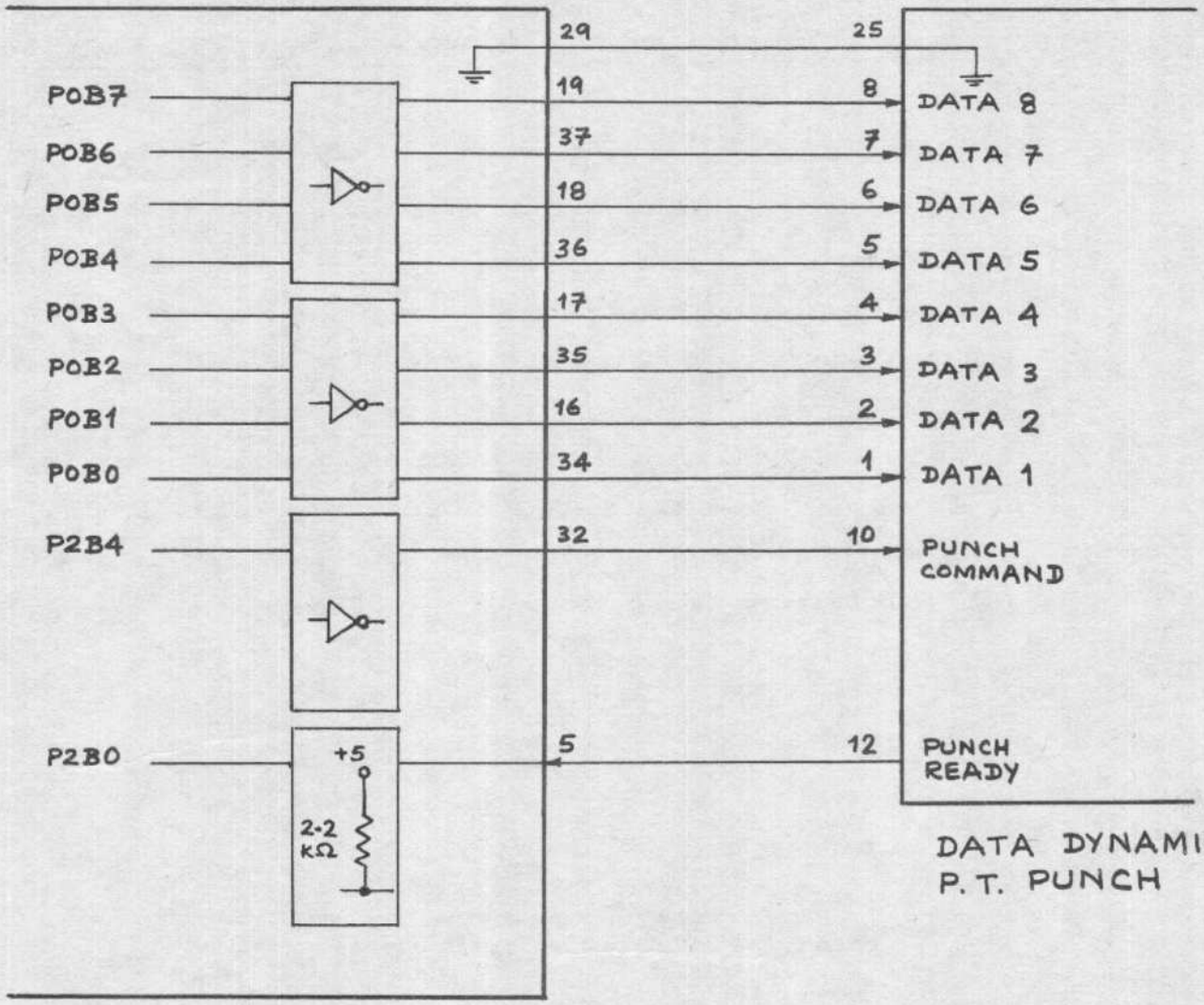


Figure 6-5 : RWC-T24 Interface to Paper-Tape Punch

6.10 MXR-4D : 4K DYNAMIC RAM MEMORY EXPANSION MODULE

6.10.1 FUNCTIONAL DESCRIPTION

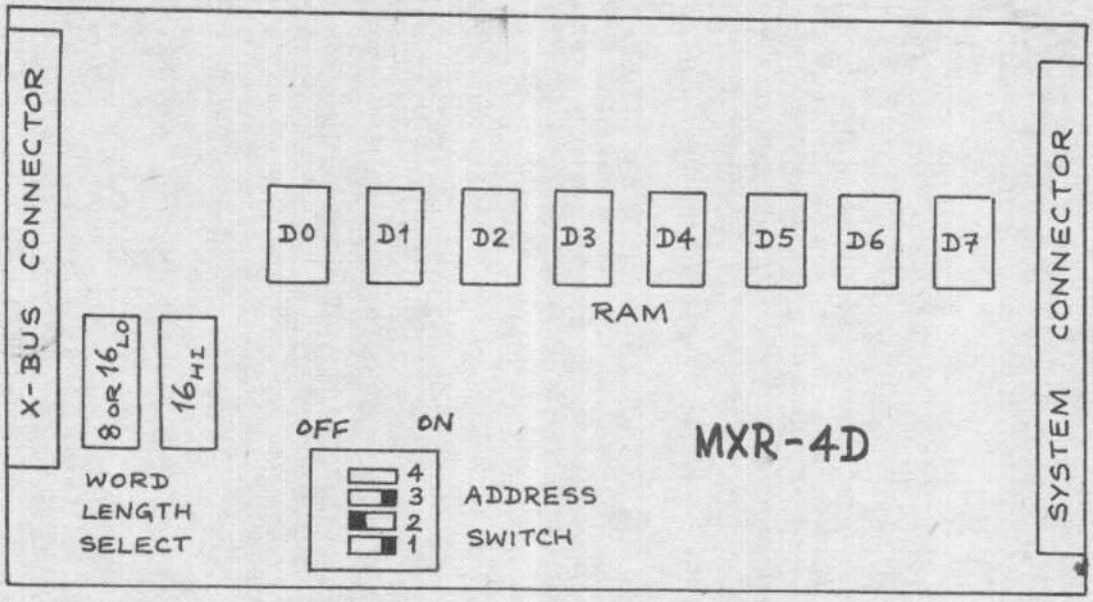
The MXR-4D module provides 4K bytes of dynamic RAM as expansion memory for DCE-X processor based systems. Automatic RAM refresh logic on the module allows the CPU on the DCE-X to run at full speed, and the memory appears just like static RAM to the user software.

An address select switch allows the RAM to occupy desired ranges in DCE-X memory address space. One or more MXR-4D modules, along with other MX memory modules, can be easily connected to a DCE-X processor via the flat-cable X-BUS connector.

6.10.2 FEATURES

- 4K byte dynamic RAM memory
- on-board refresh logic
- refresh maintained during system reset
- low power requirement
- runs at full 8080 CPU speed
- switch selectable RAM base address
- X-BUS connection to DCE-X processor module
- single 100 x 160 mm eurocard format

6.10.3 MODULE LAYOUT



6.10.4 WORD LENGTH SELECTION

The MXR-4D RAM module is designed for use with 8-bit as well as 16-bit DCE processor modules. When used with a 16-bit DCE processor, the RAM module must be assigned to either the low-order 8 bits or the high-order 8-bits of the 16-bit word. This is done by means of a component carrier which can be plugged into one of two sockets located near the X-BUS connector as shown above. When it is plugged into the left socket, the MXR-4D can be used either with an 8-bit DCE processor, or, as the low-order byte memory with a 16-bit DCE processor. When it is plugged into the right socket, the module can only be used as the high-order byte memory with a 16-bit DCE processor.

6.10.5 ADDRESS SELECTION

The RAM memory base address can be selected via a 4-bit switch located as shown in the above module layout diagram. Only the switches numbered 1 to 3 are used. Position of switch 4 is irrelevant.

The RAM base address may be set as shown on the next page.

Switch Setting 1 2 3	RAM Start Address (Hex)	RAM End Address (Hex)
On On On	0000	0FFF
Off On On	2000	2FFF
On Off On	3000	3FFF
Off Off On	4000	4FFF
On On Off	6000	6FFF
Off On Off	8000	8FFF
On Off Off	D000	DFFF
Off Off Off	A000	AFFF

Note 1 : The switch setting corresponding to start address D000 is for the DCE-X Utility system RAM (stack etc).

Note 2 : Referring to the physical module layout in Section 6.10.3 switch 1 is located towards the lower edge of the RAM card. To turn a switch on, move the switch rocker or slider to the right.

6.10.6 OPERATIONAL REQUIREMENTS

Power Requirements

The MXR-4D module requires 12V, $\pm$5V power supplies. These are obtained from the DCE-BUS via the System Connector. No other DCE-BUS signals are connected to the module.

A typical power requirement in the quiescent state is given below. Active state values are typically 20% higher.

+5V :	280 mA
-5V :	720 μA
+12V :	220 mA

Environmental Requirements

Operating temperature	:	0°C to 55°C
Storage temperature	:	-25°C to +85°C
Relative humidity	:	up to 95% noncondensing

X-BUS Drive and Load

SIGNAL	LEAKAGE	DRIVE (read data)	LOAD (write data)
Address Lines			+425μA
Data Lines	+10μA max.	+12.01mA@0.4V -2.59mA@2.4V	+10μA max.
$\overline{\text{MEMR}}$			-250μA max.
MEMW			-360μA max

Note: + indicates current into card; - indicates current out of card.

6.10.7 ORDERING INFORMATION

MXR-4D : Standard Version

The X-BUS(n) cable for connection between DCE-X and 'n' (1 to 8) memory modules must be ordered separately.

6.11 MXR-8D : 8K DYNAMIC RAM MEMORY EXPANSION MODULE

6.11.1 FUNCTIONAL DESCRIPTION

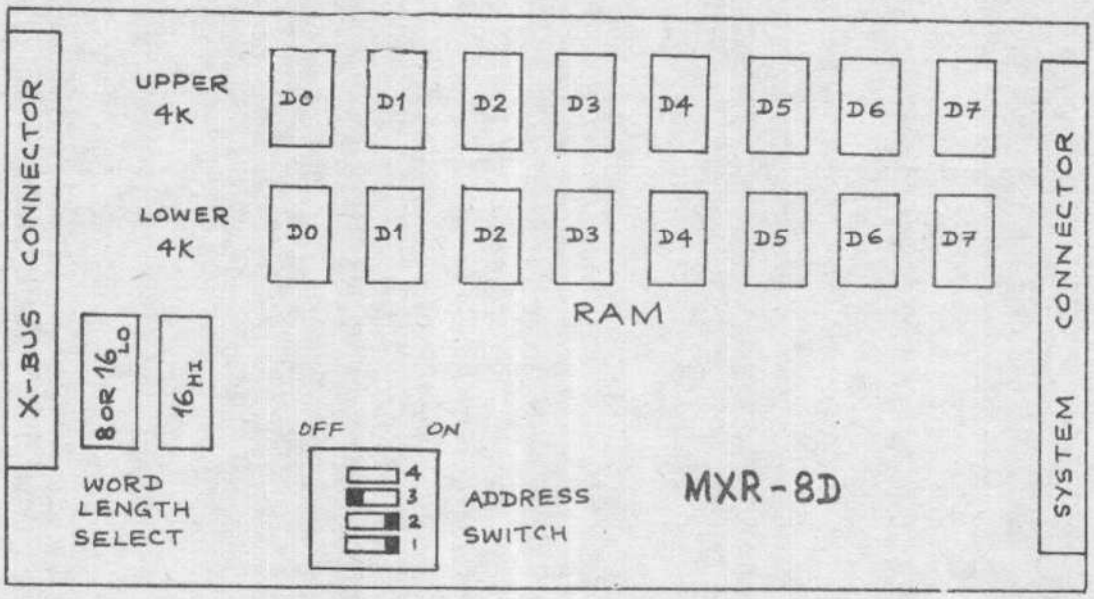
The MXR-8D module provides 8K bytes of dynamic RAM as expansion memory for DCE-X processor based systems. Automatic RAM refresh logic on the module allows the CPU on the DCE-X to run at full speed, and the memory appears just like static RAM to the user software.

An address select switch allows the RAM to occupy desired ranges in DCE-X memory address space. One or more MXR-8D modules, along with other MX memory modules, can be easily connected to a DCE-X processor via the flat-cable X-BUS connector.

6.11.2 FEATURES

- 8K byte dynamic RAM memory
- on-board refresh logic
- refresh maintained during system reset
- low power requirement
- runs at full 8080 CPU speed
- switch selectable RAM base address
- X-BUS connection to DCE-X processor module
- single 100 x 160 mm eurocard format

6.11.3 MODULE LAYOUT



6.11.4 WORD LENGTH SELECTION

The MXR-8D RAM module is designed for use with 8-bit as well as 16-bit DCE processor modules. When used with a 16-bit DCE processor, the RAM module must be assigned to either the low-order 8-bits or the high-order 8-bits of the 16-bit word. This is done by means of a component carrier which can be plugged into one of two sockets located near the X-BUS connector as shown above. When it is plugged into the left socket, the MXR-8D can be used either with an 8-bit DCE processor, or, as the low-order byte memory with a 16-bit DCE processor. When it is plugged into the right socket, the module can only be used as the high-order byte memory with a 16-bit DCE processor.

6.11.5 ADDRESS SELECTION

The RAM memory base address can be selected via a 4-bit switch located as shown in the above module layout diagram. Only the switches numbered 1 to 3 are used. Position of switch 4 is irrelevant.

The RAM address may be set as shown on the next page.

Switch Setting 1 2 3	RAM Start Address (Hex)	RAM End Address (Hex)	Possible Usage
On On On	0000	1FFF	RAM at 0 for DCE-LSA
Off On On	2000	3FFF	Above 8K PROM
On Off On	3000	4FFF	Above 12K PROM
Off Off On	4000	5FFF	Above 16K RAM (MXR-16D)
On On Off	6000	7FFF	Above 24K PROM (2 x MXP-12
Off On Off	8000	9FFF	Above 32K RAM (MXR-32D)
On Off Off	0000 D000	0FFF DFFF	For running DCE-X, 1A or 2A software on a DCE-LSA development system
Off Off Off	C000	DFFF	Above 16K + 32K RAM

Note 1: The switch setting corresponding to start addresses 0000 and D000 is for the DCE-X Utility system RAM (stack etc).

Note 2 : Referring to the physical module layout in Section 6.11.3 switch 1 is located towards the lower edge of the RAM card. To turn a switch on, move the switch rocker or slider to the right.

6.11.6 OPERATIONAL REQUIREMENTS

Power Requirements

The MXR-8D module requires 12V, $\pm$5V power supplies. These are obtained from the DCE-BUS via the System Connector. No other DCE-BUS signals are connected to the module.

A typical power requirement in the quiescent state is given below. Active state values are typically 20% higher.

+5V : 280 mA
-5V : 1440 μA
+12V : 225 mA

Environmental Requirements

Operating temperature	:	0°C to 55°C
Storage temperature	:	-25°C to +85°C
Relative humidity	:	up to 95% noncondensing

X-BUS Drive and Load

SIGNAL	LEAKAGE	DRIVE (read data)	LOAD (write data)
Address Lines			+425μA
Data Lines	+20μA max.	+12.02mA@0.4V -2.58mA@2.4V	+20μA max.
$\overline{\text{MEMR}}$			-250μA max.
MEMW			-360μA max.

Note: + indicates current into card; - indicates current out of card.

6.11.7 ORDERING INFORMATION

MXR-8D : Standard version

The X-BUS(n) cable for connection between DCE-X and 'n' (1 to 8) memory modules must be ordered separately.

6.12 MXR-16D : 16K DYNAMIC RAM MEMORY EXPANSION MODULE

6.12.1 FUNCTIONAL DESCRIPTION

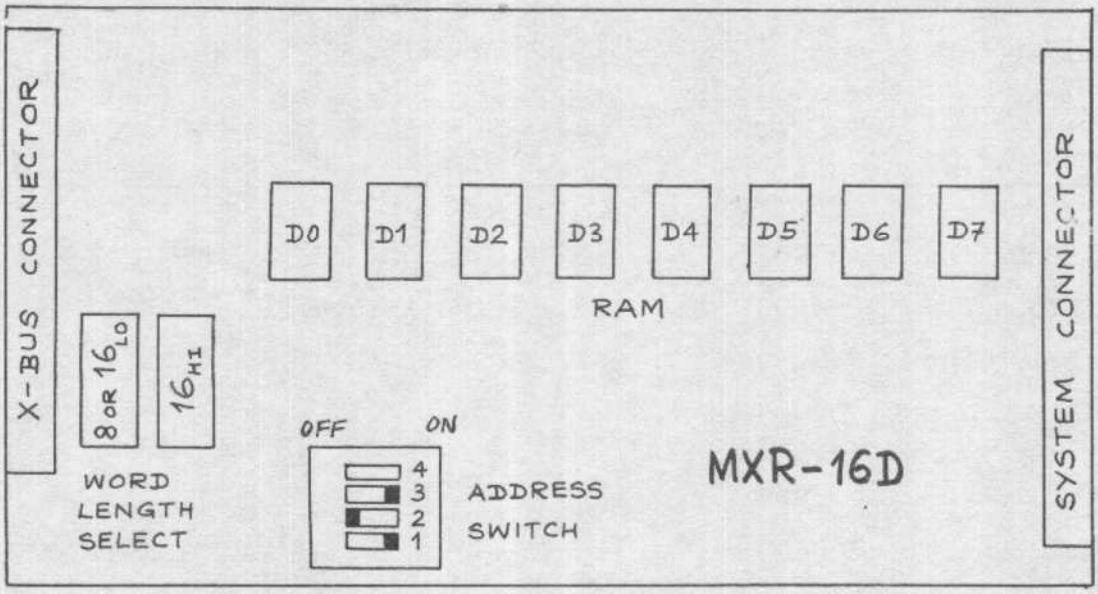
The MXR-16D module provides 16K bytes of dynamic RAM as expansion memory for DCE-X processor based systems. Automatic RAM refresh logic on the module allows the CPU on the DCE-X to run at full speed, and the memory appears just like static RAM to the user software.

An address select switch allows the RAM to occupy desired ranges in DCE-X memory address space. One or more MXR-16D modules, along with other MX memory modules, can be easily connected to a DCE-X processor via the flat-cable X-Bus connector.

6.12.2 FEATURES

- 16K byte dynamic RAM memory
- on-board refresh logic
- refresh maintained during system reset
- low power requirement
- runs at full 8080 CPU speed
- switch selectable RAM base address
- X-BUS connection to DCE-X processor module
- single 100 x 160 mm eurocard format

6.12.3 MODULE LAYOUT



6.12.4 WORD LENGTH SELECTION

The MXR-16D RAM module is designed for use with 8-bit as well as 16-bit DCE processor modules. When used with a 16-bit DCE processor, the RAM module must be assigned to either the low-order 8-bits or the high-order 8-bits of the 16-bit word. This is done by means of a component carrier which can be plugged into one of two sockets located near the X-BUS connector as shown above. When it is plugged into the left socket, the MXR-16D can be used either with an 8-bit DCE processor, or, as the low-order byte memory with a 16-bit DCE processor. When it is plugged into the right socket, the module can only be used as the high-order byte memory with a 16-bit DCE processor.

6.12.5 ADDRESS SELECTION

The RAM memory base address can be selected via a 4-bit switch located as shown in the above module layout diagram. Only the switches numbered 1 to 3 are used. Position of switch 4 is irrelevant.

The RAM address may be set as shown on the next page.

Switch Setting 1 2 3	RAM Start Address (Hex)	RAM End Address (Hex)	Possible Usage
On On On	0000	3FFF	RAM at 0 for DCE-LSA
Off On On	2000	5FFF	Above 8K PROM
On Off On	3000	6FFF	Above 12K PROM
Off Off On	4000	7FFF	With 2nd MXR-16D, or 16K PROM
On On Off	6000	9FFF	Above 24K PROM
Off On Off	8000	BFFF	With MXR-32D 32K RAM module
On Off Off	0000 D000	2FFF DFFF	For running DCE-X, 1A or 2A software on a DCE-LSA development system
Off Off Off	B000	EFFF	Highest position

Note 1 : The switch setting corresponding to start address D000 is for the DCE-X Utility system RAM (stack etc).

Note 2 : Referring to the physical module layout in Section 6.12.3, switch 1 is located towards the lower edge of the RAM card. To turn a switch on, move the switch rocker or slider to the right.

6.12.6 OPERATIONAL REQUIREMENTS

Power Requirements

The MXR-16D module requires 12V, $\pm$5V power supplies. These are obtained from the DCE-BUS via the System Connector. No other DCE-BUS signals are connected to the module.

A typical power requirement in the quiescent state is given below. Active state values are typically 20% higher.

+5V : 280 mA
-5V : 55 mA
+12V : 220 mA

Environmental Requirements

Operating temperature	:	0°C to 55°C
Storage temperature	:	-25°C to +85°C
Relative humidity	:	up to 95% noncondensing

X-BUS Drive and Load

SIGNAL	LEAKAGE	DRIVE (read data)	LOAD (write data)
Address Lines			+425μA
Data Lines	-10μA to +10μA	12.01mA max.@0.4V -2.61mA max.@2.4V	-10μA to +10μA
$\overline{\text{MEMR}}$			-250μA max.
MEMW			-360μA max.

Note: + indicates current into card; - indicates current out of card.

6.12.7 ORDERING INFORMATION

MXR-16D : Standard Version

The X-BUS(n) cable for connection between DCE-X and 'n' (1 to 8) memory modules must be ordered separately.

6.13 MXR-32D : 32K DYNAMIC RAM MEMORY EXPANSION MODULE

6.13.1 FUNCTIONAL DESCRIPTION

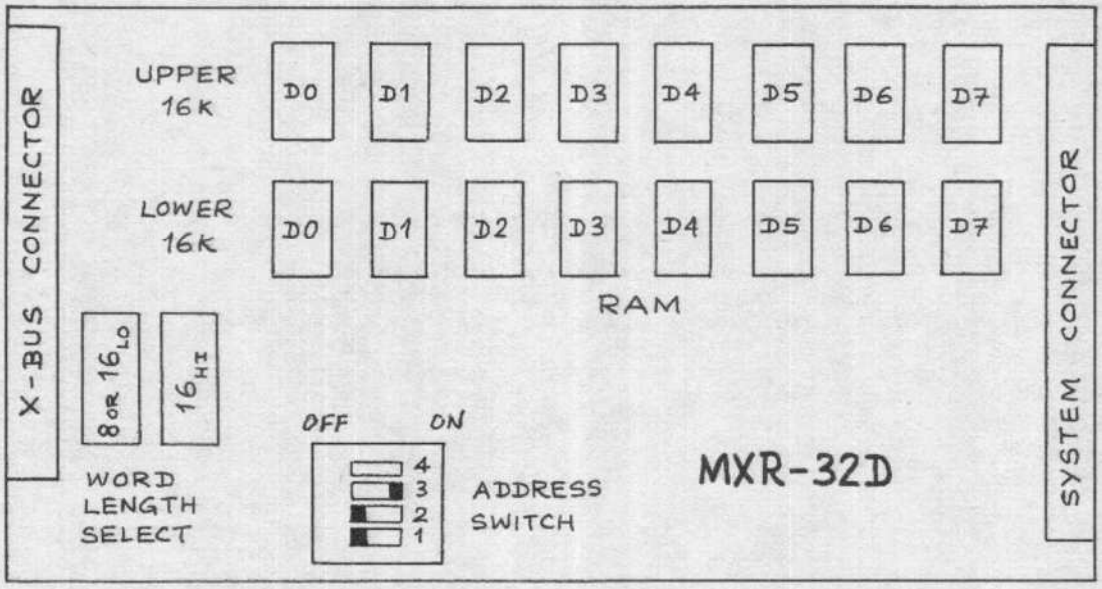
The MXR-32D module provides 32K bytes of dynamic RAM as expansion memory for DCE-X processor based systems. Automatic RAM refresh logic on the module allows the CPU on the DCE-X to run at full speed, and the memory appears just like static RAM to the user software.

An address select switch allows the RAM to occupy desired ranges in DCE-X memory address space. Upto two MXR-32D modules along with other MX memory modules, can be easily connected to a DCE-X processor via the flat-cable X-BUS connector.

6.13.2 FEATURES

- 32K byte dynamic RAM memory
- on-board refresh logic
- refresh maintained during system reset
- low power requirement
- runs at full 8080 CPU speed
- switch selectable RAM base address
- X-BUS connection to DCE-X processor module
- single 100 x 160 mm eurocard format

6.13.3 MODULE LAYOUT



6.13.4 WORD LENGTH SELECTION

The MXR-32D RAM module is designed for use with 8-bit as well as 16-bit DCE processor modules. When used with a 16-bit DCE processor, the RAM module must be assigned to either the low-order 8-bits or the high-order 8-bits of the 16-bit word. This is done by means of a component carrier which can be plugged into one of two sockets located near the X-BUS connector as shown above. When it is plugged into the left socket, the MXR-32D can be used either with an 8-bit DCE processor, or, as the low-order byte memory with a 16-bit DCE processor. When it is plugged into the right socket, the module can only be used as the high-order byte memory with a 16-bit DCE processor.

6.13.5 ADDRESS SELECTION

The RAM memory base address can be selected via a 4-bit switch located as shown in the above module layout diagram. Only the switches numbered 1 to 3 are used. Position of switch 4 is irrelevant.

The RAM address may be set as shown on the next page.

Switch Setting 1 2 3	RAM Start Address (Hex)	RAM End Address (Hex)	Possible Usage
On On On	0000	7FFF	RAM at 0 for DCE-LSA
Off On On	2000	9FFF	Above 8K PROM
On Off On	3000	AFFF	Above 12K PROM
Off Off On	4000	BFFF	Above 16K RAM
On On Off	6000	DFFF	Above 24K PROM
Off On Off	1000	8FFF	Above 4K PROM
On Off Off	0000 D000	6FFF DFFF	For running DCE-X, 1A or 2A software on a DCE-LSA development system
Off Off Off	8000	EFFF	With 2nd MXR-32D and DCE-LSA

Note 1 : The switch setting corresponding to start address D000 is for the DCE-X Utility system RAM (stack etc).

Note 2 : Referring to the physical module layout in Section 6.13.3 switch 1 is located towards the lower edge of the RAM card. To turn a switch on, move the switch rocker or slider to the right.

6.13.6 OPERATIONAL REQUIREMENTS

Power Requirements

The MXR-32D module requires +12V, $\pm$5V power supplies. They are obtained from the DCE-BUS via the System Connector. No other DCE-BUS signals are connected to the module.

A typical power requirement in the quiescent state is given below. Active state values are typically 20% higher.

+5V : 280 mA
-5V : 110 mA
+12V : 230 mA

Environmental Requirements

Operating temperature	:	0°C to 55°C
Storage temperature	:	-25°C to +85°C
Relative humidity	:	up to 95% noncondensing

X-BUS Drive and Load

SIGNAL	LEAKAGE	DRIVE (read data)	LOAD (write data)
Address Lines			+425μA
Data Lines	-20μA to +20μA	12.02mA max.@0.4V -2.62mA max.@2.4V	-20μA to+20μA max.
$\overline{\text{MEMR}}$			-250μA max.
MEMW			-360μA max.

Note: + indicates current into card; - indicates current out of card.

6.13.7 ORDERING INFORMATION

MXR-32D : Standard Version

The X-BUS(n) cable for connection between DCE-X and 'n' (1 to 8) memory modules must be ordered separately.

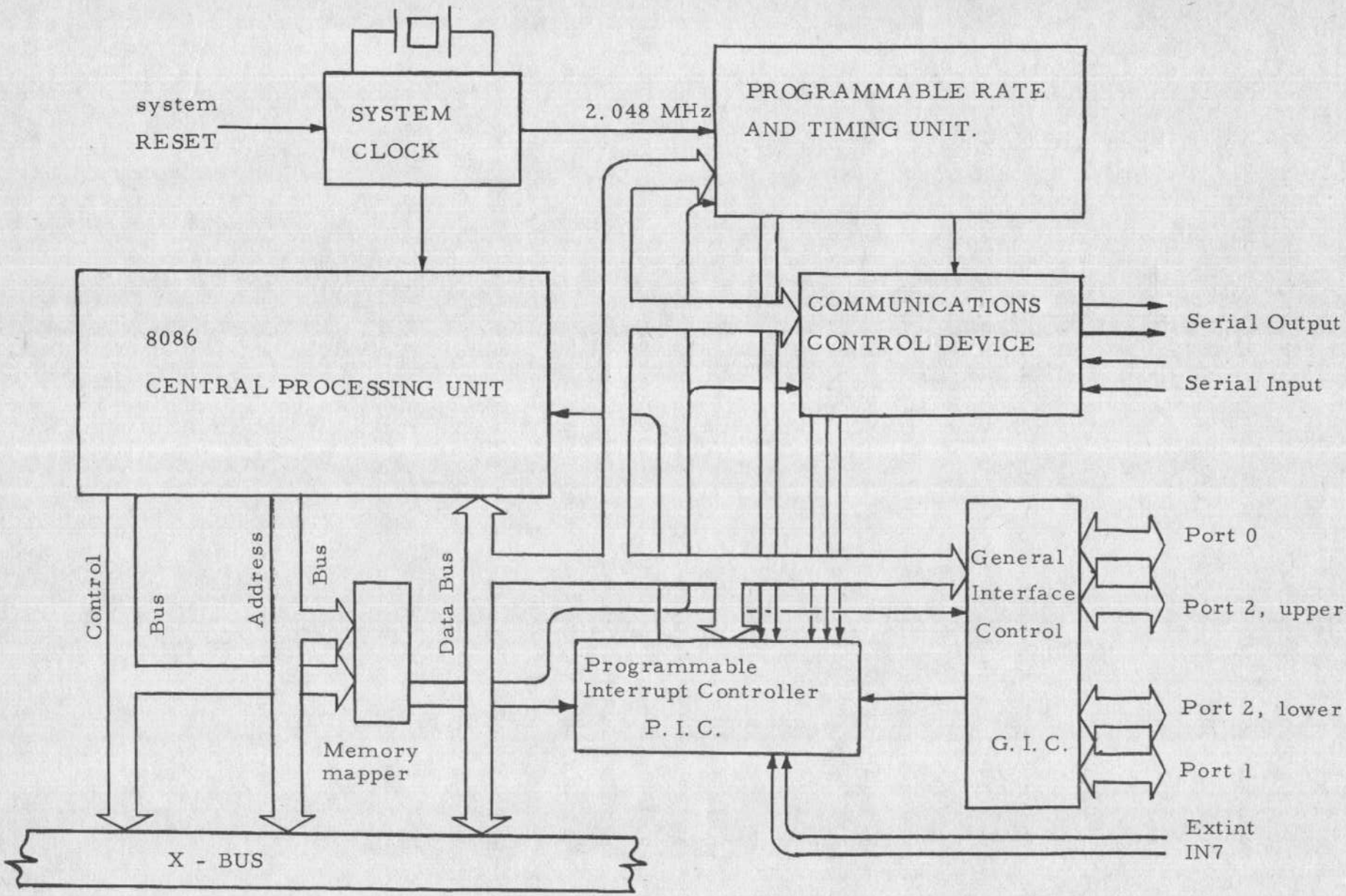
6.14 DCE-X86 16-BIT PROCESSOR MODULE

6.14.1 FEATURES

- Complete 8086, 16 bit microcomputer system on a single 100 x 160 mm eurocard.
- 2K byte RAM and sockets for 4K or 8K byte EPROM.
- Memory expandable with upto 60K x 16-bit via flat-cable X-Bus.
- Opto-isolated serial I/O with programmable baud rates.
- Synchronous, asynchronous, and isosynchronous modes.
- 24 parallel I/O lines, programmable as simple, handshaking or bi-directional with automatic handshake control signals.
- Hardware support for DAI's "fast-bus" transfer mode.
- 2 independent interval timers providing 500 nano-second resolution, with crystal accuracy.
- Advanced interrupt controller, provides both simple and rotating priority modes.
- Instructions to manipulate 8 and 16-bit words, including hardware multiply and divide.
- 3 external interrupt lines.

The DCE-X86 is a single eurocard format microcomputer module incorporating the 8086 highspeed 16-bit microprocessor. It provides the user the possibility of combining the software power of this microprocessor together with the complete interface capabilities provided by the family of DCE-BUS compatible modules.

The DCE-X86 module can be used either as a single card microcomputer, or, by the addition of compatible memory expansion modules, it becomes a central processing and system controller module. The memory space provided can be translated into a high address field, thus leaving all low address space (from zero) free for the memory expansion modules.



DCE-X86: Functional Block Diagram

(Memory not shown)

In addition to the microprocessor and memory facilities, the DCE-X86 module also provides a total system control architecture. This includes a centralised interrupt controller, programmable serial input and output interfaces, and a timer-counter group. The following sections will describe them in more detail, including the necessary software aspects related to each in turn.

6.14.2 Memory

The DCE-X86 module provides the user both RAM and EPROM memory, thus enabling its application as a stand-alone controller. However, this can be augmented by a collection of memory expansion cards. The on-card memory will then be used as stack/workspace (RAM) and Utility/Bootstrap (EPROM). All Addresses from 00000H upto 1DFFFH are then left free for the memory expansion modules (120K bytes).

In order to release the memory at low address space, commencing with address zero (necessary for the operation of the 8086 device), an optional memory configuration is provided. This must be ordered specifically at the time of purchase and is only required if the module is to have memory expansion attached.
All of the peripheral devices found on the eurocard are included into the 8086 memory space. The addresses relative to each device, and also for the memory, are defined in the following table:

Memory Segment Number	Address Bits 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	Description
0	0 0 0 0	A A A A	A A AA	AAAA	AAAB	32K + 32K byte system memory
1A	0 0 0 1	0 A A A	A A AA	AAAA	AAAB	16K + 16K byte system memory
1B	0 0 0 1	1 0 A A	A A AA	AAAA	AAAB	8K + 8K byte system memory
1C	0 0 0 1	1 1 0 A	A A AA	AAAA	AAAB	4K + 4K byte system memory
1D	0 0 0 1	1 1 1 X	X X XX	XXXX	XXXX	DO NOT USE
3	0 0 1 1	1 1 1 X	X X XX	XXXX	XXA0	Communications control
5	0 1 0 1	1 1 1 X	X X XX	XXXX	XAA0	Timing and Rate Controller
7	0 1 1 1	1 1 1 X	X X XX	XXXX	XAA0	General Interface controller
9	1 0 0 1	1 1 1 X	X X XX	XXXX	XXA0	Programmable interrupt controller
B	1 0 1 1	1 1 1 X	X A AA	AAAA	AAAB	RAM with optional memory mapper
F	1 1 1 1	1 1 1 C	A A AA	AAAA	AAAB	2716/2732 EPROM memory
0A	0 0 X X	X X X X	X A AA	AAAA	AAAB	RAM with memory map supplied.

Notes:

A = Memory address line
B = Bank select address controls both A_0/8086 and $\overline{BHE}$.
C = Ø for 2716 devices or Address line for 2732's.
X = Don't care.

DON'T use EVEN segments (with the exception of segment zero)!

Memory arrangement for DCE-X86 microcomputer module.

6.14.3 Memory Organisation

The 8086 microprocessor manipulates data transfers to and from memory over 2 independant 8-bit data busses. These relate to a high and low byte of a 16 bit data-word. It is therefore possible, so long as an even address is selected, to read or write a full 16 bits with only one memory cycle. The two data busses share a common memory cycle. 16 bit memory access can occur with anODD address, but they need 2 cycles for execution bits. Available at the X-Bus connector, the X-Bus addresses now form 8086 address A1 through A16. AØ is used to select the low byte memory bank, whilst a special signal, $\overline{\text{BHE}}$, is used to select the high bank of memory. In 16 bit transfers these two signals can simultaneously become active. Also organised on the X-Bus cable, and supported by DAI's family of dynamic RAM memory expansion modules, are 8 extra databus lines. The memory modules can be connected either to the high or low databus lines as required. The same memory module cannot, however, be split between both data lines.

The on-card EPROM memory is organised as 1 chip per bus. All peripheral devices reside on the low byte bus.

6.14.4 Programmable Interrupt Controller

The device employed on the DCE-X86 module enables the user to select the system responses to the available interrupts.

Eight system interrupt lines are supported. These are known as INØ to IN7. Normally, INØ will have the highest priority, and IN7 the lowest. This priority order can be influenced by commands from the user. The assignment of functions to each of these interrupt lines is as follows:

INØ	EXTINT	System bus interrupts
IN1	INT7	
IN2	GIC	
IN3	TIMER 2	
IN4	TIMER 1	
IN5	Receive Buffer full	Serial Interface Interrupts.
IN6	Transmit Buffer Empty	
IN7	Break or Sync. Detect.	

Internal to the interrupt controller, there are 3 important registers. They operate closely together and have the following functions.

a) Interrupt Request Register (IRR)

This register provides one bit for each of the interrupt lines. A bit is set whenever the related interrupt exhibits the condition required to request an interrupt. This condition may be either level or edge sensitive. The selection of which is made during the software initialisation.

b) Interrupt Mask Register (IMR)

Each interrupt request input can be individually masked by the Interrupt Mask Register, (IMR), programmed by the user. Each bit in the IMR masks one interrupt channel if it is set to 1. Bit Ø masks IRØ, bit 1 masks IR1 and so forth. Edge-triggered interrupts during the time that an interrupt is masked will cause a service request when the mask is removed. Thus, if the interrupt mask is used to selectively ignore interrupts, care must be taken to trap these supurious requests.

c) Interrupt Service Register (ISR)

These register bits become set when the 8086 microprocessor acknowledges an interrupt. This is normally performed by hardware, and is thus transparant to the user. In response to the interrupt acknowledgement, the bit corresponding to the highest request priority will be set in the ISR, and the corresponding bit in the IRR will be reset. Only requests which are

unmasked will be considered for service. The service request register normally masks off requests from interrupts of lower priority. This feature can be disabled by supplying a suitable operations command to the controller. This is described in section 6.14.4.5 under the title "special mask mode".

The appropriate bit in the ISR will remain set until a suitable End of Interrupt command is given to the controller. Unmasked interrupts of higher priority can still cause an interrupt of the service routine. Thus, more than one bit may be set in the ISR allowing for several interrupt service routines to be nested.

6.14.4.1 Initialisation procedure

The user must always initialise the interrupt controller before any interrupts can be processed. If required, initialisation can occur more than once. This is useful when the application demands a change of the fundamental operation of the controller.

Three important parameters are transferred to the controller during the initialisation sequence. There are defined by the code values of three successive bytes which are to be sent to the controller device. The device employed is the 8259A interrupt controller. Manufacturers' documentation relating to this device mentions a large collection of operating modes. These each have a mnemonic associated with every command word issued to the device. Those commands chosen are listed, together with their mnemonic codes for reference.

Mnemonic	Address	Data	Description
ICW1 I	9FFF0	X X X 1 0 X 1 1	Select edge trigger
ICW1 J	9FFF0	X X X 1 1 X 1 1	Select level sense
ICW2	9FFF2	V V V V V X X X	Issue vector
ICW4 B	9FFF2	0 0 0 0 0 0 0 1	Programmed EOI
ICW4 D	9FFF2	0 0 0 0 0 0 1 1	Automatic EOI

Notes:

X Don't care

0,1 Literal 0 or 1

VVVVV 5 bit vector

Table 1. Initialisation command words

The normal mode of operation is for the interrupts to be edge triggered. Level sense mode will cause a continuous interrupt request if the corresponding interrupt is not removed before an end of interrupt (EOI) is issued.

Never use Level sense mode if either interrupts IN2,5,6, or 7 are enabled.

ICW1 must be issued, and always followed by ICW2 and ICW4 before any other communication with the controller device can commence.

ICW2 defines the address block used by the 8086 to carry the entry points of all of the interrupt service routines. This 5 bit value is multiplied by 32 to define the entrypoint for IN0. All of the other interrupt entry points follow successively at 4 byte intervals. The 4 bytes provided for each interrupt allows for a set Interrupt Instruction (STI , to enable interrupt servicing of higher priority interrupts), followed by a suitable JUMP or CALL instruction.

A call instruction is useful for IN5 (Receive buffer full). The consequence of this is to immediately follow with transmit character service routine. This echoes the received character back to the attached console device.

The first 4 vector fields (VVVVV = 0,1,2,or3) are reserved for future DAI Software. The user is advised to use vectors other than these. Vector field Ø can also conflict with the internal trap vectors of the 8086 (e.g. trap if division by zero).

ICW4 specifies if the device should operate in the Automatic End of Interrupt mode (AEOI). When this mode is selected, the ISR bit will be reset immediately the service routine is entered. Thus, the device can immediately register requests for interrupt from all of the unmasked lines. If AEOI mode is used, the interrupts of the 8086 should not be reenabled until the 8086 instruction, IRET (Interrupt Return), restores the Interrupt Enable Flag into the flag registers.

6.14.4.2 End of Interrupt Processing and Priority Control

In applications which use several of the available System Interrupts, it is often advantageous to use the programmed end of interrupt mode of operation. This command is available in several different forms. These are given in the following table:

Mnemonic	Address	Data	Description
OCW2 E	9FFF0	0 0 1 0 0 0 0 0	Reset bit of highest priority set in ISR.
OCW2 SE	9FFF0	0 1 1 0 0 n n n	Reset bit in ISR corresponding to IN'n'
OCW2 RE	9FFF0	1 0 1 0 0 0 0 0	Reset bit of highest priority in ISR and assign this interrupt to the lowest priority level.
OCW2 RSE	9FFF0	1 1 1 0 0 n n n	Reset bit in ISR corresponding to IN'n' and assign interrupt to the lowest priority level.

OCW2 R	9FFF0	0 1 0 0 0 0 0 0	Enable automatic assignment to lowest priority level if in AEOI mode.
OCW2 CR	9FFF0	0 0 0 0 0 0 0 0	Disable automatic assignment of lowest priority if in AEOI mode.
OCW2 RS	9FFF0	1 1 0 0 0 n n n	Assign IN'n' as lowest priority. Does not affect ISR.

Table 2. End of Interrup Command Group.

The specific end of interrupt commands (OCW2 SE and RSE) are normally used when the service routine sequence disturbs the normal nesting of the interrupt requests. Thus, a low priority interrupt service routine can be completed from within the service routine for an interrupt operating on a higher level.

The current priority status can be modified under program control. The function of the rotating priority commands in the EOI command Group (OCW2 SE through RS) is to define the interrupt request of lowest priority. This is usual to be the request that was last serviced. The relative priorities of all of the other interrupt requests are implicitly defined by the lowest priority assignment.

Interrupt assigned to lowest priority	Interrupt requests in ascending priority	Notes
IN0	0 - 7 - 6 - 5 - 4 - 3 - 2 - 1	
IN1	1 - 0 - 7 - 6 - 5 - 4 - 3 - 2	
IN2	2 - 1 - 0 - 7 - 6 - 5 - 4 - 3	
IN3	3 - 2 - 1 - 0 - 7 - 6 - 5 - 4	
IN4	4 - 3 - 2 - 1 - 0 - 7 - 6 - 5	
IN5	5 - 4 - 3 - 2 - 1 - 0 - 7 - 6	
IN6	6 - 5 - 4 - 3 - 2 - 1 - 0 - 7	
IN7	7 - 6 - 5 - 4 - 3 - 2 - 1 - 0	Assignment at RESET

The priority status can be modified at any time, without affecting the content of the ISR, by issuing the command OCW2 RS.

6.14.4.3 Communication with the Internal Registers of the Programmable Interrupt Controller.

After initialisation, it is necessary to write the required mask byte into the IMR (Interrupt Mask Register). This register is initially reset to unmask all interrupts. Thus, the interrupts not required for service must be selectively masked.

The Interrupt Mask Register can normally be written to at any time after initialisation by executing a memory write to address 9FFF2.

The content of the mask register can also be read by executing a memory read from address 9FFF2.

The other status registers, IRR and ISR, can be exclusively read from address 9FFF0. Unless otherwise initialised, a status read will provide the user the current content of the IRR (Interrupt Request Register). Selection and deselection of the ISR can be made by issuing a special command word to address 9FFF0. These are as follows:

Mnemonic	Address	Data	Description
OCW3 RIS	9FFF0	0 0 0 0 1 0 1 1	Select ISR
OCW3 RR	9FFF0	0 0 0 0 1 0 1 0	Deselect ISR

Table 3. Status Register Select Group

It is not necessary to repeat these command words before the execution of every status read. The interrupt controller will always return the content of the current selected register.

6.14.4.4 Polled Interrupts - Their philosophy and implementation

It is sometimes necessary to be able to operate an interrupt priority structure under control of the operational program. When this interrupt method is used, the microprocessor shall not respond to an interrupt request. The interrupt controller will then wait for a software interrupt acknowledgement sequence. The user must first issue a poll request command. This is as follows:

Mnemonic	Address	Data	Description
OCW3 P	9FFF0	0 0 0 0 1 1 0 0	Poll, request status.

All of the interrupt requests will now be frozen at the current requesting priority (if one exists). A subsequent status read from address 9FFF0 will now reveal one of two conditions:

a) 0 X X X X X X X No interrupt active

b) 1 X X X X n n n Interrupt "nnn" requesting service.

If an interrupt is indicated by the polled status, its corresponding bit in the IRR is cleared, and set in the ISR. The ISR responds as normal to the End of Interrupt Group of commands.

6.14.4.5 Special Mask Mode

Normally, and following initialisation, an interrupt level currently being serviced (ISR bit set) will automatically mask requests from all interrupts of lower priority. This feature can be disabled and reenabled by the following two commands:

Mnemonic	Address	Data	Description
0CW3 SM	9FFF0	0 1 1 0 1 0 0 0	Set special mask mode
0CW3 RSM	9FFF0	0 1 0 0 1 0 0 0	Reset special mask mode

Special Mask Mode - commands

6. 14. 4. 6 Conclusion

The Programmable Interrupt Controller provides the user an extremely powerful control structure. The above section describes all of the functional commands relating to its application on the DCE-X86 module. Examination of a manufacturers' documentation for the device will reveal an extended set of possible commands relating to other applications for this particular device. The user is thus recommended to confine himself to the description given above in order to avoid any confusion with this device.

6.14.5 Communications Control Device

The serial communications capability is provided by a USART (Universal Synchronous/Asynchronous Receiver and Transmitter) type n° 8251A. This device is functionally identical to that described in the chapter on the RWC-CCE interface module.

The USART registers appear as memory addresses to the 8086 microcomputer. These addresses, which may be either read from or written to, are as follows:

Address	Description
3F000	Transmit or Received data
3F002	Mode/Command or Status.

Communications Device Addressing.

The device is first initialised by writing the required mode and command bytes to address 3F002. The same address can then be read, to establish status, and data transferred either to or from the device by using address 3F000. Details of this initialization and execution sequence is given on page 7-126 of this manual, under the sections entitled "USART Devices for channel 1 and 2". The reader must be sure not to be confused with the different register addressing found in those chapters, and also to remember that the RWC-CCE documentation describes a module that includes 2 USART devices.

6.14.5.1 Communications device connector.

The assignment of the signals on this connector is different from that found on the DCE-1, -2, -X family of modules. Several signal definitions have been changed in order to exploit the operational advantages of the communications control device.

The following pin definitions are valid for the DCE-X86 processor module:

SIGNAL NAME	DESCRIPTION	PIN
SOPOS	Serial Output (Positive)	21
SONEG	Serial Output (Negative)	22
SIPOS	Serial Input (Positive)	17
SINEG	Serial Input (Negative)	18
$\overline{DSR}$	Data set Ready	1
$\overline{CTS}$	Clear to send	4
TxC	Transmit clock input	5
RxC	Receive clock input	6
CkOUT	Serial clock output	7
TxD	Transmit data - TTL	2
RxD	Received data - TTL	3
+12V	+12V from system connector	14
+5V	+5V from system connector	15
-5V	-5V from system connector	16
GND	Signal and supply ground	19

The connector fitted to the module is a 25 pin D-type male.

Under usual operating conditions, the clock connections (pins 5, 6, and 7) are connected together by user selectable jumpers provided on the module. These jumpers are fitted to all standard DCE-X86 modules. The individual connections are present to enable either synchronous or isosynchronous communication methods to be employed.

TTL level signals of the transmitted and received data are available. These enable communications to be made at rates above 9600 bauds. Opto-isolated communications can only be made at transmission rates at or below 9600 bauds. The maximum rate allowed with these TTL signal lines is 50k Baud. Modem handshake lines are provided for the control of character transmission. Received characters must ALWAYS be handled by the application program. No control for the received communications is provided.

6.14.5.2 Serial Interface - Interrupts

The serial communications interface is supported by 3 of the system's interrupts. Two of these, "Transmit buffer empty" and "Receive buffer full" are also found on the other DCE cards which employ the TICC device. In addition, a special interrupt is provided for.
This interrupt, SYNC/BREAK detect, causes a request for system interrupt whenever a specific condition occurs. When programmed to use asynchronous communications, the communications device will cause an interrupt request whenever a break condition occurs. Thus, the break key on the attached terminal device can be used to cause a specific system interrupt. This feature is employed in DAI Support software and is used to cause a return to the system utility program.

When communications are being made with synchronous communication, this interrupt will occur whenever the receiver detects a valid synchronisation code. This interrupt will then be used to ready the receive character routines to receive a block of data. By using a suitable application program, high-level communications protocols including BSC can therefore be supported by the DCE-X86 module.

6.14.6 Programmable Rate and Timing device

This device is identical to that employed in DAI's RWC-CCE module. However, the assignment of functions to each of the three timer-counters is dedicated as follows:

Timer counter 0 : Communications rate generator. Connected to device connector pin 7.
Timer counter 1 : Interrupting system timer. Connected to interrupt controller.
Timer counter 2 : idem.

A full description of this device, the 8253A, is found under the sections relating to the RWC-CCE module. Exceptions to this however are as follows:

6.14.6.1 8253A Addressing

The 8253A device can be selected at the following hexadecimal addresses.

Address	Description
5F000	Counter 0, read or write
5F002	Counter 1, read or write
5F004	Counter 2, read or write
5F006	Write mode word.

Note: DO NOT read from location 5F006.

6.14.6.2 8253A Modes

Each of the three timer-counters of the 8253A can be selected to operate in any one of six possible pulse or waveform modes. Under the normal operating conditions applied to the DCE-X86 module, the following modes are used:

Channel	Function	Mode select byte	
		Binary	BCD
0	Baud rate generator	36	37
1	Timer	70	71
2	Timer	B0	B1

Timers 1 and 2 can also be programmed to perform a repeating timer interrupt function. This is selected by writing the following mode select bytes:

Channel	Function	Mode select byte	
		Binary	BCD
1	Repeating timer	74	75
2	Repeating timer	B4	B5

In all cases, a required count is written to the selected timer by the following sequence:

(i) Send "Mode select byte" to mode address.

(ii) Send least significant 8 bits followed by most significant 8 bits to selected counter address.

In all cases, the counters, each of 16 bit operation, can be selected to operate in either a binary or BCD (Binary Coded Decimal) count-down format.

The timers are also provided with an extra 16 bit register. This can be loaded with the current count of any of the 3 counters by issuing one of the following mode select bytes to address 5F006.

Counter	Mode Select byte to latch count
0	00
1	40
2	80

Following the issuance of one of these bytes, the next two read operations from the selected counter will reveal first the least and then the most significant bytes of the latched counter.

In order to reset the internal operation of the device, it is necessary to perform two dummy read operations from each counter (see RWC-CCE section, page 7-132).

6.14.6.3 Baudrate generation

In order to generate any of the standard Baud rates used for serial communications, a correct 16 bit count value must be loaded for the operation of counter-timer 0. In order to acheive rate errors of less than 5 %, the following table of hexadecimal count values has been prepared. The counter is to be operated in the binary mode.

Baud rate required	Count values (Hexadecimal) x1	x16	x64
45	B1C7	0B1C	02C7
50	A000	0A00	0280
75	6AAB	06AB	01AB
110	48BA	048C	0123
134,5	3B7B	03B8	00EE
150	3555	0355	00D5
200	2800	0280	00A0
300	1AAB	01AB	006B
600	0D55	00D5	0035
1200	06AB	006B	001B
2400	0355	0035	000D
4500	01AB	001B	0007
9600	00D5	000D	-
19200	006B	0007	-

Note: Both high and low bytes MUST be written to the device, even when high byte is zero.

6.14.6.4 Timing calculation

The count frequency, common to all three timer-counters, is 2.048 MHz. Thus, the period for each count is approximately 500 ns.

6.14.7 16-bit, X-BUS DESCRIPTION

In order to support the extended data and address requirements of the DCE-X86 module, the following pin allocations have been made.

Pin number	Name	Description
1	D8	16 bit data-bus
2	D0	
3	D9	
4	D1	
5	D10	
6	D2	
7	D11	
8	D3	
9	D12	
10	D4	
11	D13	
12	D5	
13	D14	
14	D6	
15	D15	
16	D7	
17	$\overline{BHE}$	High bank enable D8-D15
18	AO-86	Low bank enable D0-D7

19	GROUND	
20	MEMW	Memory write strobe
21	GROUND	
22	N. C.	
23	A.11	Address line 11
24	$\overline{\text{MEMR}}$	Memory read strobe
25	A15	Address lines
26	A12	
27	A13	
28	A14	
29	A10	
30	A16	
31	A8	
32	A9	
33	A6	
34	A7	
35	A4	
36	A5	
37	A2	
38	A3	
39	A1	
40	INTA	Interrupt acknowledge
41	GROUND	
42	$\overline{\text{WRQ}}$	Wait cycle request
43	N. C.	
44	N. C.	
45	GROUND	
46	$\overline{\text{HOLDA}}$	Hold acknowledgement
47	N. C.	
48	CK2(TTL)	CPU clock, phase 2.
49	$\overline{\text{HOLD}}$	Hold request
50	ALE	Address latch enabled.

Notes:

1. The signal names are left tabulated if they are standard X-BUS assignments, and right-tabulated if unique to the DCE-X86 module.
2. N.C. No connection.

6.14.8 Operational Requirements

Power Requirements

The DCE-X86 module requires three power supplies. These are usually provided by the DCE system power supply module via the DCE-BUS. Typical power requirements in the quiescent state are given below. Active state values are typically 20 % higher.

+12V	$\pm$ 5%
+5V	$\pm$ 5%
-5V	$\pm$ 5%

Environmental requirements

Operating temperature	: 0°C to 55°C
Storage temperature	: -25°C to +85°C
Relative humidity	: 95% non-condensing.

6.14.9 ORDERING INFORMATION

DCE-X86	: Standard DCE-X86 module with provision for 2716 device EPROMS.
DCE-X86/S	: Same as DCE-X86, but with 8086 socket mounted.
DCE-X86A	: DCE-X86 module with provision for 2732 device EPROMS.
DCE-X86A/S	: Same as DCE-X86A, but with 8086 socket mounted.

All of the above versions are fitted with the standard memory mapper (RAM at address 0) and software DCE-BUS mode operation.

Optionally, the following modules can be ordered:

X86-MAP	Optional memory mapper, places RAM at address B0000.
X86-FBUS	Optional FAST-BUS hardware handshake module.

Interface cables for standard terminals and memory expansion must be ordered separately.