2. GENERAL INTERFACE CONTROL (GIC)

The two most important features of the DCE are that it makes optimum use of the available I/O pins and the interrupts are software definable. Therefore, it is possible to provide interface logic for almost any I/O device without the need for additional external logic or components. The multifunction input-output terminals allow the designer to tailor the DCE to the interface characteristics of the connected peripheral devices. This section details the GIC features and explains how to use software to "fit" the DCE to applications with parallel data I/O requirements.

2.1 PARALLEL INPUT-OUTPUT

Section 6.1.4 details the pin assignments of the 31 pin System Connector. 24 pins of this connector are devoted to parallel data communications through three 8-bit general interface ports: PORT 0, PORT 1, and PORT 2. These ports are general-purpose data channels configured under the direction of the General Interface Control. Through selected bits or groups of bits of these ports, the user can input or output data directly to or from the CPU. Software controls the selection of bits and the modes of I/O according to the possibilities listed in Section 2.7.2.

Group A of Section 2.7.2 refers to the alternative modes that can be used to input or output data through PORT 0 and the four "upper" bits (4 to 7) of PORT 2. Group B refers to I/O modes through PORT 1 and the four "lower" bits (0 to 3) of PORT 2. A specific configuration from groups A and B can be selected with the instruction of general format: "GICC Amode, Bmode". For example, the instruction "GICC 1,2" sets all 8 bits of PORT 0 in output mode, all 8 bits of PORT 1 in input mode, all 4 "upper"

bits of PORT 2 in input mode, and all 4 "lower" bits of PORT 2 in output mode. The "GICC 1,2" in this example is a GIC Configuration Command. The Configuration Commands are usually executed during the initialization of the DCE. GICC is a macro instruction.

A configuration command can be followed by a compatible GIC I/O command listed in Section 2.7.3. For example, if the macro command "STGI 0" follows the "GICC 1,2" instruction, the GIC will write the 8-bit word in the 8080 accumulator to PORT 0. After a Configuration Command several I/O Commands may occur in the program, provided they are compatible with the configuration established for the specific ports.

In modes 0 through 3 in both groups the input and output operations are simple; data is simply written to or read from a specified port; no handshaking is required. While the outputs in these modes are latched, the inputs are not. Data written to an output port is latched by the port and may be read back with the "LDGI" instruction (see Section 2.7.3) as if it were stored in RAM memory location. Note also, that in these modes PORT 2 is used simply to transfer data to or from peripheral devices just like ports 0 and 1. Figures 2-1 and 2-2 show the simple input and output modes.

Output data latched in the GIC ports can be handled as if they were stored in memory locations since each port has a specific address as shown on the Memory and Register Diagram in figure 6-2. For example, if the H and Lregister pair of the 8080 holds the address 1C00H of the PORT 0, then the "INR M" instruction will increment the data held in PORT 0. Thus a counter can be set up directly in the GIC port referenced by the H and L register pair.

When a Configuration Command specifies a handshake mode (H. S.), the handshake control signals(H. C. S.) pass through specified bits of PORT 2 as indicated in the following Sections. The input handshake control signals are defined in Figure 2-3 and in Section 2. 2, and the output handshake signals are defined in Figure2-4 and in Section 2. 3. PORT 0 handshake control signals are provided by PORT 2 upper bits, while PORT 1 handshake control signals are provided by PORT 2 lower bits.

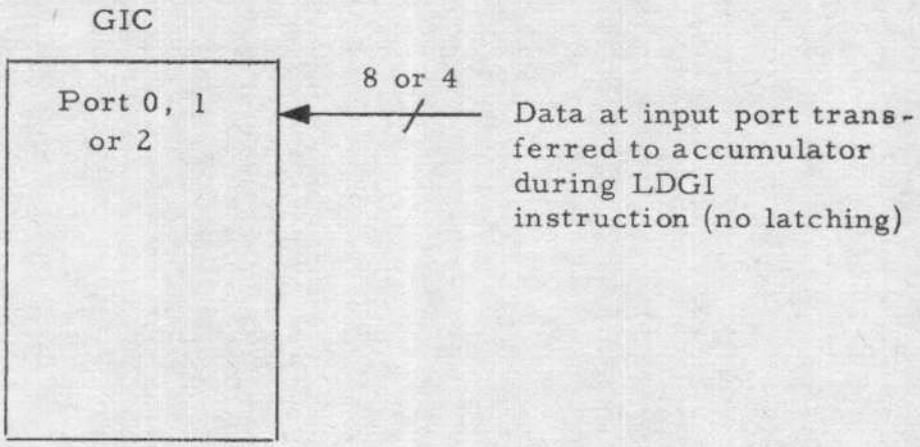


Figure 2-1. GIC Port Function: Input Mode

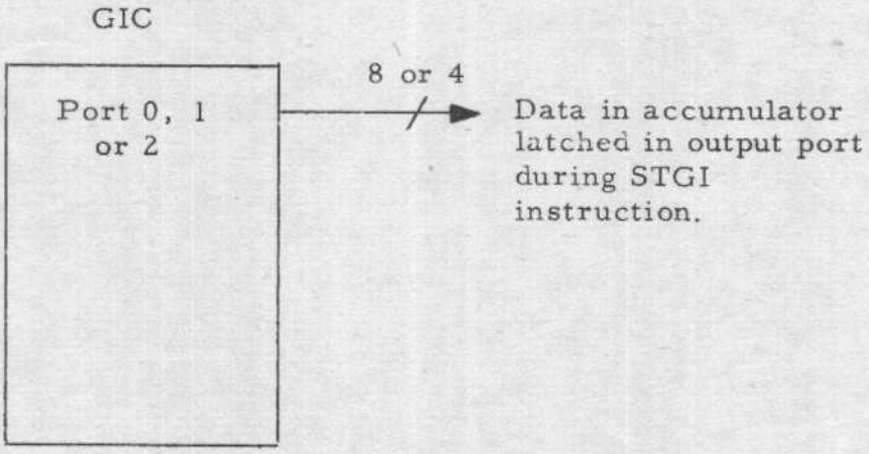


Figure 2-2. GIC Port Function: Output Mode

2.2 INPUT HANDSHAKE CONTROL SIGNALS (see figure 2.3)

$\overline{STB}$ (Strobe Input)

Apply to PORT 2 bit 4 for input data at PORT 0, and to PORT 2 bit 2 for input data at PORT 1.

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full)

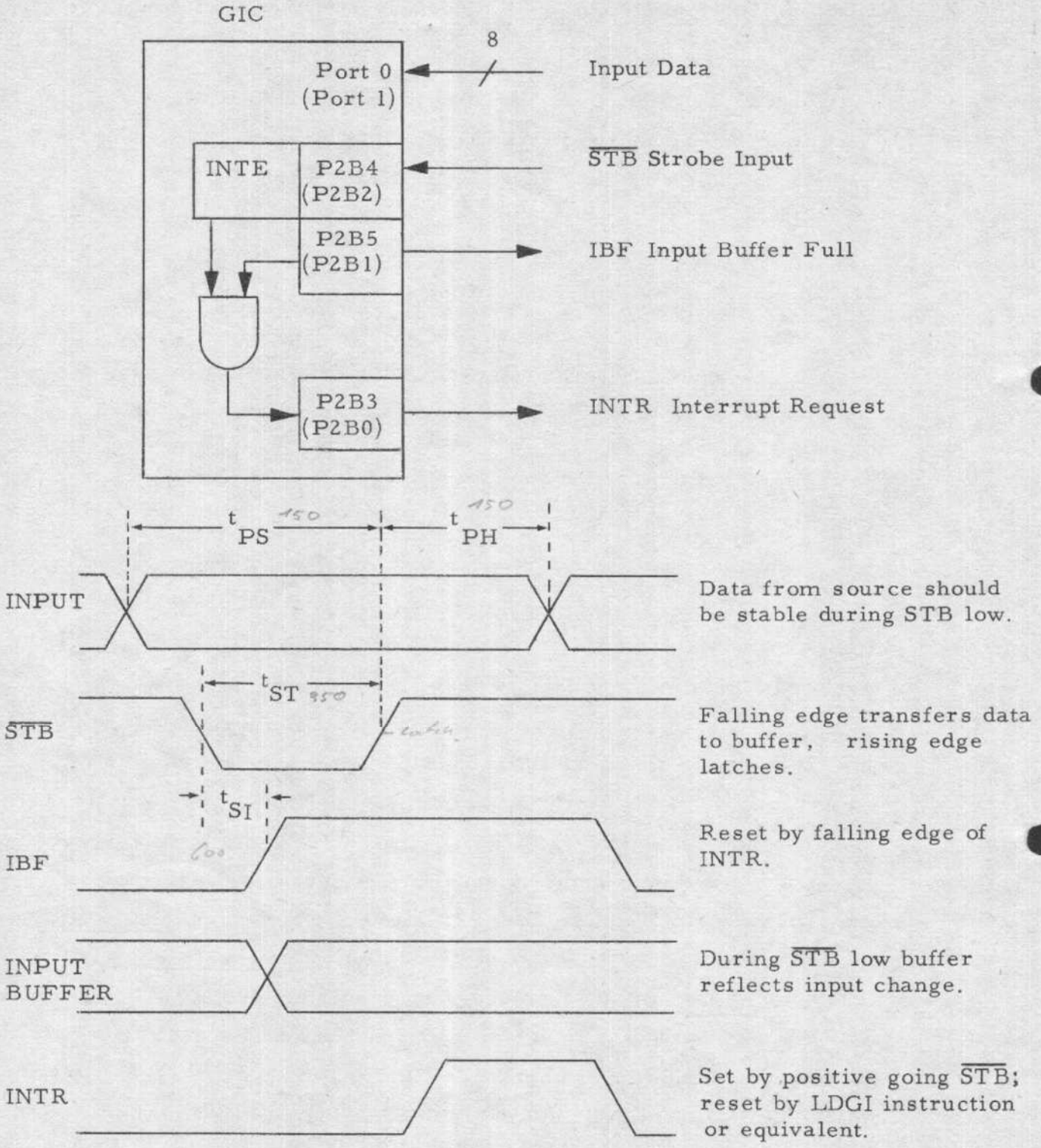
Appears on PORT 2 bit 5 for input data at PORT 0, and on PORT 2 bit 1 for input data at PORT 1.

A "high" on this output acknowledges to the data source that the data has been loaded into the input latch and no new data should be sent until this output returns to low.

INTR (Interrupt Request)

Appears on PORT 2 bit 3 for input data at PORT 0, and on PORT 2 bit 0 for input data at PORT 1.

A "high" on this output indicates to program that an input device has strobed its data into the port. Thus, the programmer can allow a specific input device to interrupt the CPU by simply strobing data into the port. To achieve this condition he must connect the INTR output to the EXINTR input, or to the IN7 (auxiliary interrupt) input on the device or system connector. Having the INTR output hard wired to one of the external interrupts, the programmer can still enable or inhibit interrupts with the program. The INTR output indicating data at PORT 0, is blocked if bit 4 of PORT 2 is at logical ZERO, and it is passed if this bit is at logical ONE. Therefore, by setting bit 4 of PORT 2 "high" with the instruction "BSET 4" the interrupt condition is enabled. Clearing this bit with the instruction "BCLR 4" disables the interrupt condition. (The instructions "BSET 2" and "BCLR 2" enable or inhibit interrupts with respect to data at PORT 1). These bits can be written to, even though they are used for the input strobe $\overline{STB}$. The interrupt modes are also disabled by a new GIC configuration command.



NOTE: For time parameter values see Section 2.6.2

Figure 2-3 Port Function: Handshaking Input Mode (Latching)

2.3 OUTPUT HANDSHAKE CONTROL SIGNALS (see figure 2-4)

$\overline{OBF}$ (Output Buffer Full)

Appears on PORT 2 bit 7 for output data at PORT 0, and on PORT 2 bit 1 for output data at PORT 1.

A "low" condition on this output indicates that data has been transferred from the 8080 CPU to the output buffer. The falling edge of the $\overline{ACK}$ input signal resets this output to the high condition.

$\overline{ACK}$ (Acknowledge Data Received)

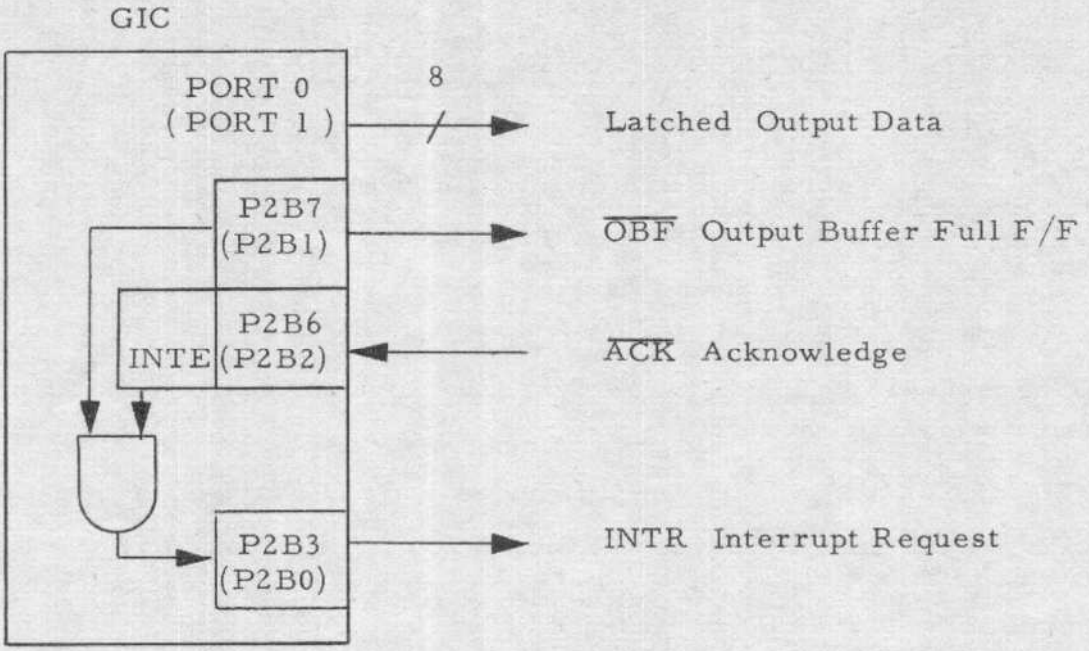
Apply this input to PORT 2 bit 6 for data received from PORT 0 and to PORT 2 bit 2 for data received from PORT 1.

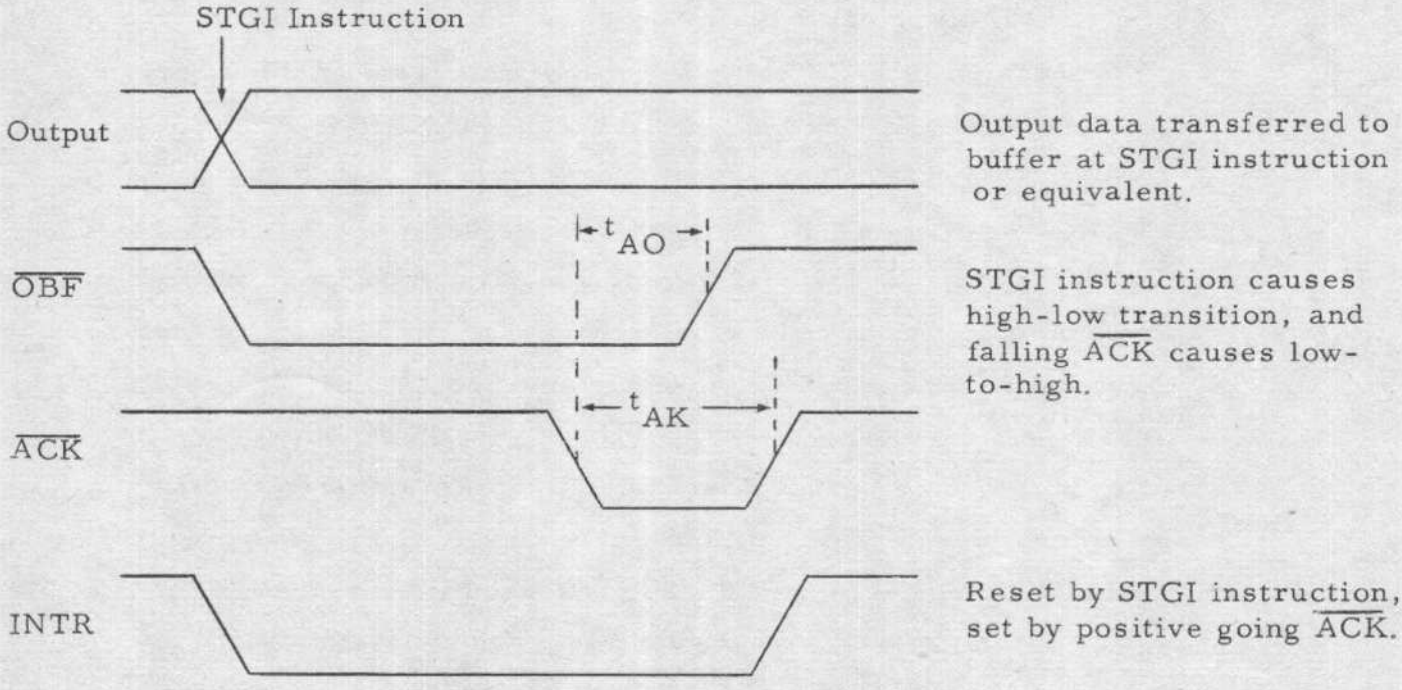
A "low" on this input indicates to the DCE that the peripheral device accepted the data from PORT 0 or PORT 1.

INTR (Interrupt Request)

Appears on PORT 2 bit 3 for output data from PORT 0, and on PORT 2 bit 0 for output data from PORT 1.

A "high" on this output indicates that a peripheral device has accepted data from the port. Thus, the programmer can allow a peripheral device to interrupt the CPU by simply accepting data from the port. To achieve this condition, he must connect the INTR output to the EXINTR input, or to the IN7 (auxiliary interrupt) input on the device or system connector. Having the INTR output hard wired to one of the external interrupts, the programmer can still enable or inhibit interrupts with the program. The INTR output, indicating data taken from PORT 0, is blocked if bit 6 of PORT 2 is at logical ZERO, and it is passed if this bit is at logical ONE. Therefore, by setting bit 6 of PORT 2 "high" with the instruction "BSET 6" the interrupt condition is allowed. Clearing this bit with the instruction "BCLR 6" disables the interrupt condition. (The instructions "BSET 2" and "BCLR 2" enable or inhibit interrupts with respect to data taken from PORT 1). These bits can be written to, even though they are used for input strobe $\overline{ACK}$. The interrupt modes are also disabled by a new GIC configuration command.





NOTE: For time parameter values see Section 2.4.2

Figure 2-4 GIC Port Function: Handshaking Output Mode

There are several combination of modes where not all of the bits in PORT 2 are used for handshake control signals. These bits, if configured as inputs, will transfer data to the CPU when "LDGI 2" or equivalent is executed. However, if they are programmed as outputs, the 4 "upper" bits must be individually accessed using the single-bit set/clear instructions (see Section 2.7.1); while the four lower bits (0 to 3) can be set or reset individually or accessed together by the "STGI" command or equivalent.

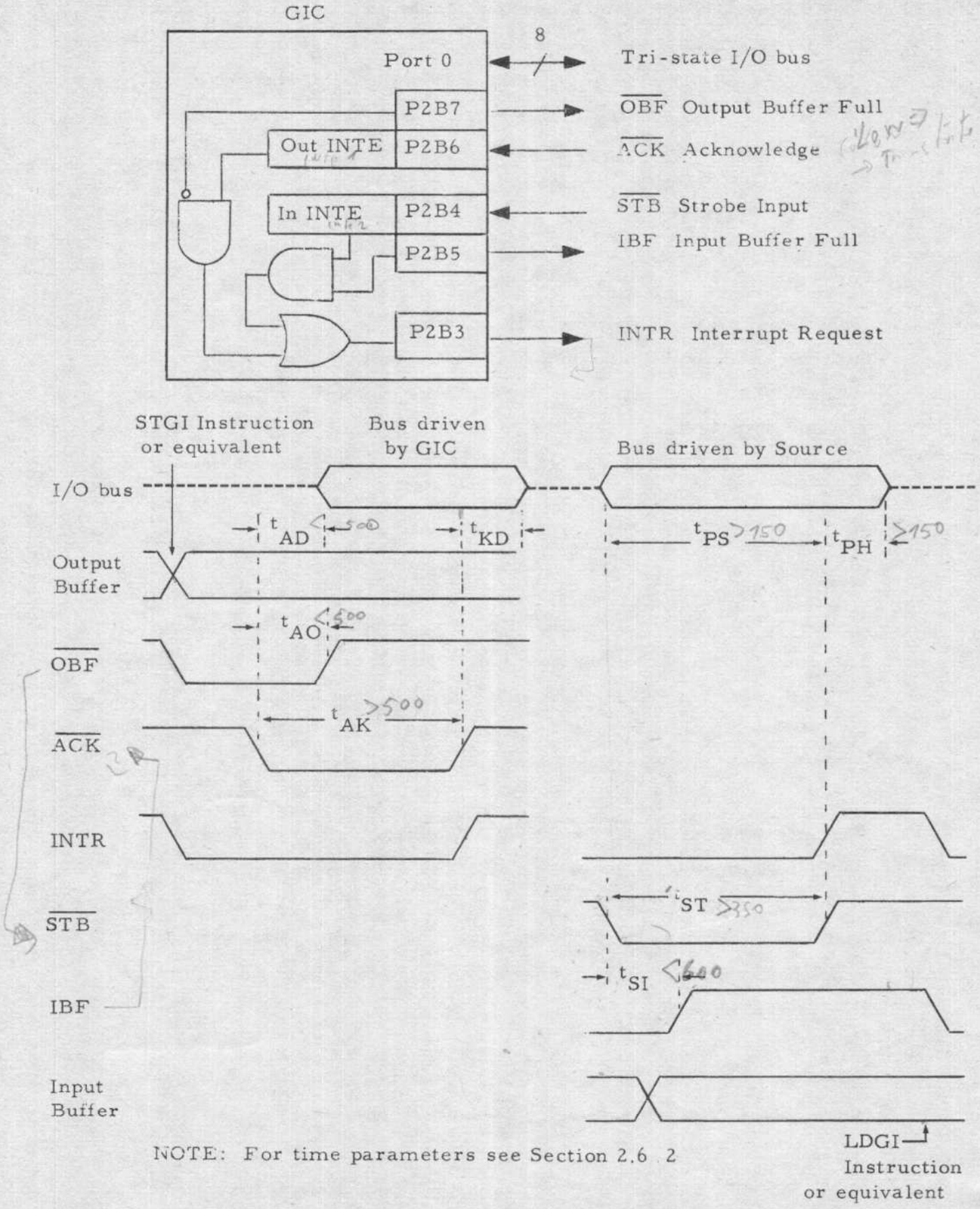
The individual set/clear capability of PORT 2 can control simple switch closing or display computational results. The DCE can also drive directly darlingtons for high voltage displays through any set of eight output buffers selected from PORTS 1 and 2; these buffers can source 1mA at 1.5 volt as required by this type of load.

2.4 BI-DIRECTIONAL I/O MODE (see figure 2-5)

MODE 8 defined in Section 2.7.2 specifies a bi-directional I/O mode. This mode is available for PORT 0 only; it provides the facilities for transmitting and receiving information to and from a peripheral device through a single 8-bit bus. Handshaking signals on bits 3, 4, 5, 6 and 7 of PORT 2 maintain the proper bus discipline. In this mode PORT 0 inputs and outputs are latched independently from each other.

The input and output handshake signals for Mode 8 are the same as described above with the exception of the $\overline{\text{ACK}}$ input. A "low" on this input puts the PORT 0 3-state output buffer in the low impedence state, enabling it to send out the data. Normally, in Mode 8, PORT 0 is in the high impedence state. See Figure 2-5 for the definition of this port function.

There are additional 8-bit parallel I/O ports on the Device Connector. These come from the TICC, and are described in Section 4.



NOTE: For time parameters see Section 2.6.2

Figure 2-5 GIC Port Function: Bi-Directional I/O Mode

2.5 SYNCHRONIZED DATA TRANSFER

The memory and register diagram of Figure 6-2 shows two addresses for PORT 0. The address 5C00 allows fast, burst-mode data transfer between the DCE and peripheral devices such as floppy disc, magnetic tape, or mass storage devices. Fast data transfer, usually performed with peripheral hardware such as DMA controller, is possible to accomplish in the DCE with the user program.

The following example illustrates how to use the synchronized mode for fast data transfer to a 256 byte memory page.

```
        LXI  H, BUFFER   ;  Point to RAM MEMORY BUFFER
        LXI  D, GICS     ;  Point to PORT 0 sync mode (5C00)
LOOP:   LDAX D           ;  Read PORT 0 sync mode
        MOV  M, A        ;  Transfer data to memory
        INR  L           ;  Increment memory block address
        JNZ  LOOP        ;  Loop until end of memory block
                            (register L content is zero)
```

In this program the LDAX instruction waits for the data to arrive to PORT 0; this condition is indicated by the rising edge of the $\overline{STB}$ pulse. Without the sync-mode port address in the register pair D, the LDAX instruction would not wait, and the CPU would be required to spend extra time to interrogate the port for the presence of the new data. In such a case the transfer of a byte from PORT 0 to RAM would take 26.5 microseconds. In the synchronous mode the software loop above takes 14.5 microseconds to complete, allowing a transfer rate of 70,000 bytes per second.

2.6 GIC PORT CHARACTERISTICS

2.6.1 D. C. Characteristics T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Cond.
V_{IL}	Input Low Voltage			.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			.4	V	Note1
V_{OH}	Output High Voltage	2.4			V	Note2
$I_{OH}(1)$	Darlington Drive Current		2.0		mA	Note3

Note 1: I_{OL} = 1.6mA
Note 2: I_{OH} = 50 μA
Note 3: V_{OH} = 1.5V, R_{EXT} = 390 Ω

2.6.2 A. C. Characteristics T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{AK}	Width of ACK Pulse	500			ns
t_{ST}	Width of STB Pulse	350			ns
t_{PS}	Set-Up Time for Peripheral	150			ns
t_{PH}	Hold Time for Peripheral	150			ns
t_{RA}	Hold Time for A_1, A_0 after RD = 1	379			ns
t_{RC}	Hold Time for CS after RD = 1	5			ns
t_{AD}	Time from ACK = 0 to Output (Mode 2)			500	ns
t_{KD}	Time from ACK = 1 to Output Floating			300	ns
t_{WO}	Time from WR = 1 to OBF = 0			300	ns
t_{AO}	Time from ACK = 0 to OBF = 1			500	ns
t_{SI}	Time from STB = 0 to IBF			600	ns
t_{RI}	Time from RD = 1 to IBF = 0			300	ns

2.7 GIC COMMANDS

2.7.1 Port 2 Bit Set/Clear Commands

Macro Instruction

BCLR nbit — clears specified bit in PORT 2

BSET nbit — sets specified bit in PORT 2

nbit = 0, 1, 2, 3, 4, 5, 6, 7

2.7.2 GIC Configuration Command

GICC amode, bmode

GROUP A MODE	PORT 0	PORT 2 (Bits affected)
0	Output	Output (4-7)
1	Output	Input (4-7)
2	Input	Output (4-7)
3	Input	Input (4-7)
4	H. S. Output	H. S. C. (3,6,7) Output (4,5)
5	H. S. Output	H. S. C. (3,6,7) Input (4,5)
6	H. S. Input	H. S. C. (3,4,5) Output (6,7)
7	H. S. Input	H. S. C. (3,4,5) Input (6,7)
8	Bi-directional	H. S. C. (3,4,5,6,7)

GROUP B MODE	PORT 1	PORT 2 (Bits affected)
0	Output	Output (0-3) +
1	Output	Input (0-3) +
2	Input	Output (0-3) +
3	Input	Input (0-3) +
4	H. S. Output	H. S. C. (0,1,2)
6	H. S. Input	H. S. C. (0,1,2)

\+ Bit 3 not affected if Group A in modes 4 through 8

In the above "Handshake" = H. S.

"Handshake Control" = H. S. C.

2.7.3 GIC I/O Commands

MACRO INSTRUCTION	DESCRIPTION	FUNCTION
LDGI 0	Parallel read of PORT 0	(A)←(PORT 0)
STGI 0	Parallel write to PORT 0	(PORT 0)←(A)
LDGIS 0	Synchronized read of PORT 0	(A)←(PORT 0) *
STGIS 0	Synchronized write to PORT 0	(PORT 0)←(A) *
LDGI 1	Parallel read of PORT 1	(A)←(PORT 1)
STGI 1	Parallel write to PORT 1	(PORT 1)←(A)
LDGI 2	Parallel read of PORT 2	(A)←(PORT 2)
STGI 2	Parallel write to PORT 2	(PORT 2)←(A) **

*Transfer synchronized with the INTR signal low-to-high transition on P2B3 (see section 2.5).

**If Group A is in mode 4 or 6, bits 4-7 can only be changed by direct bit-set or bit-clear commands.

EXAMPLE

To configure Group A in mode 7 and Group B in 0

```
GICC 7, 0
```

After this command PORT 0 will be configured as handshaking input port, with the handshake control signals passing through bits 3, 4, and 5, of PORT 2, as described in Section 2.2. Bits 6 and 7 of PORT 2 will be configured as simple input. PORT 1 and bits 0 to 3 of PORT 2 will be configured as simple outputs.

NOTE: The Macro instructions BCLR, BSET and GICC are all 5 bytes long and modify the accumulator.