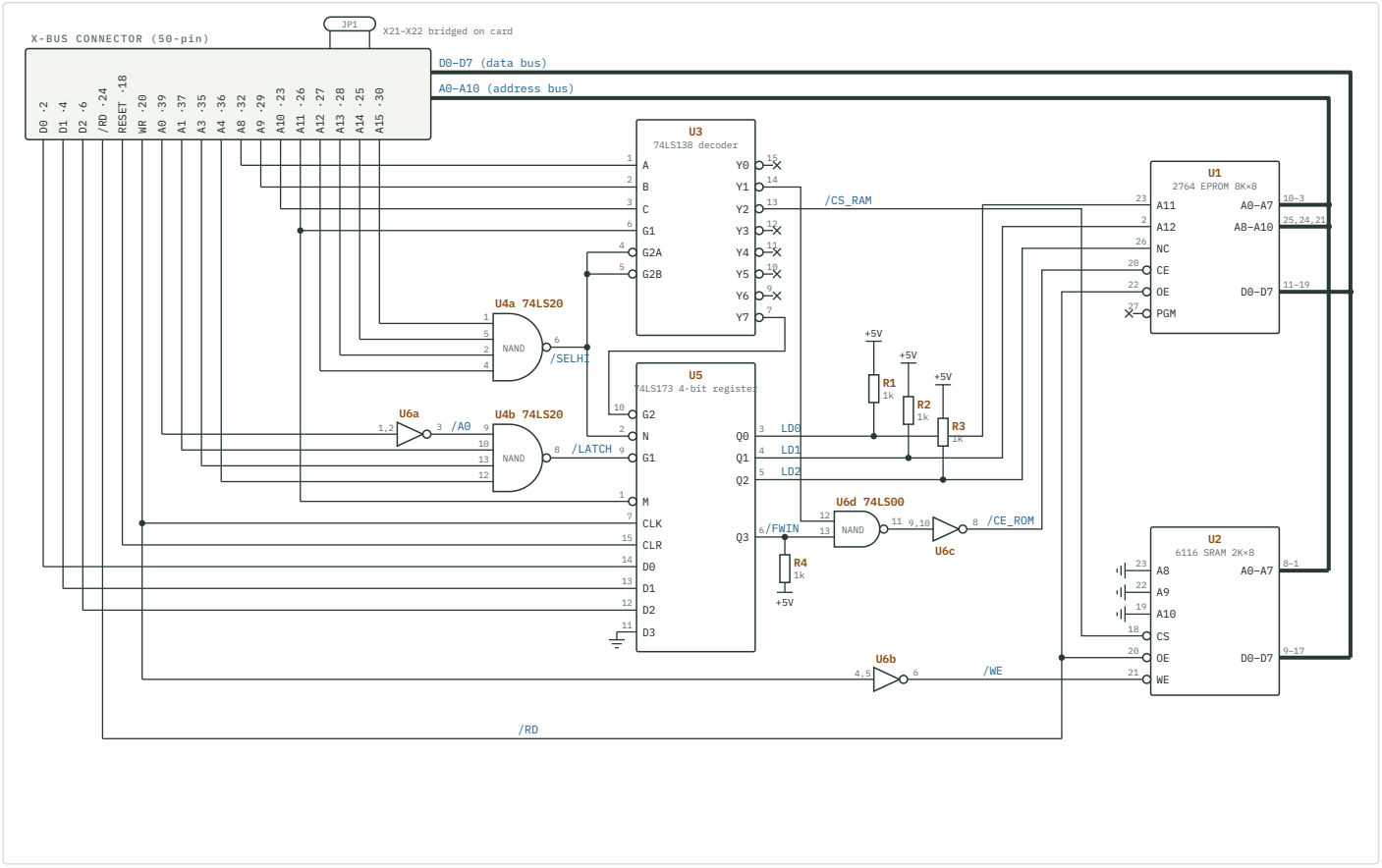
DAI PERSONAL COMPUTER · X-BUS EXPANSION · CARD "NR 1.85"

DAI-DOS 1541 X-Bus Card

Gate-level view reconstructed from continuity traces and tests on the running DAI (netlist rev AB). Every connection is drawn as a wire; dots mark junctions, crossings without a dot are not connected. Thick lines are the 8-bit data and 11-bit address buses. Small grey numbers are IC pin numbers; bubbles mark active-low pins.



ADDRESS MAP

CPU RANGE	SELECTED BY	DEVICE
F000–F7FF	U5 outputs enabled (A11 = 0, /SELHI = 0); Q3 (/FWIN) = 0 enables U1	2764, bank = U5 Q1,Q0 → EPROM A12,A11
F900–F9FF	U3 Y1	2764 offset 1900–19FF (LD0, LD1 pulled high = bank 3)
FA00–FAFF	U3 Y2	6116, 256 bytes (A8–A10 grounded)
FFxx write, A0 = 0, A1 = A3 = A4 = 1	U3 Y7 and /LATCH, clocked by WR	U5 loads D0–D2 = bank (e.g. FFFE)
F800–F8FF, FB00–FEFF	Y0, Y3–Y6 not connected	left to the mainboard (stack RAM, 9511, I/O)

EQUATIONS

- `/SELHI = ¬(A15·A14·A13·A12)`
- `/LATCH = ¬(¬A0·A1·A3·A4)`
- `U3 enabled = A11 · ¬/SELHI`, outputs Y = A10..A8
- `U5 load = WR↑ · ¬/LATCH · ¬/Y7`; reset clears to bank 0
- `U5 output enable = ¬A11 · ¬/SELHI`
- `/CE_ROM = /Y1 · /FWIN` (/FWIN = U5 Q3: 0 in F000–F7FF, pulled high by R4 otherwise)
- `/WE = ¬WR` (6116 gated by its own /CS)

CONFIDENCE

- All decode and control pins shown are traced by continuity; the bank behaviour is confirmed on the DAI (period 4, bank 3 F100 page = F900 page).
- U1 A0–A7, D0–D7 and U2 A0–A7, D0–D7 are assumed straight to the bus; the dumps decode as coherent 8080 code and the RAM works.
- Four 1 kΩ pull-ups to +5 V: R1, R2, R3 on LD0–LD2 (EPROM A11, A12, pin 26) and R4 on /FWIN (U5 pin 6 → U6 pin 13). WR (X-bus 20) has no pull-up; it is driven by the mainboard. Confirmed on the board 2026-10-15.
- U1 pin 26 (LD2) is not connected inside a 2764, so latch bit D2 has no effect. Power pins and decoupling are not drawn.
- The X-bus reset line (pin 18) is the added wire from 8255 pin 35, as described in the DAI-DOS 1541 installation instructions.